

MODEL NAME : **EDW40**

PCB NO : **LA-H451P**

BOM P/N : **451AFX31L01 (DIS I3 4G)**
451AFX31L02 (DIS I3 8G)
451AFX31L03 (DIS I3 16G)
451AFX31L04 (DIS I5 4G)
451AFX31L05 (DIS I5 8G)
451AFX31L06 (DIS I5 16G)
451AFX31L07 (DIS I7 4G)
451AFX31L08 (DIS I7 8G)
451AFX31L09 (DIS I7 16G)
451AFX31L10 (UMA I3 4G)
451AFX31L11 (UMA I3 8G)
451AFX31L12 (UMA I3 16G)
451AFX31L13 (UMA I5 4G)
451AFX31L14 (UMA I5 8G)
451AFX31L15 (UMA I5 16G)
451AFX31L16 (UMA I7 4G)
451AFX31L17 (UMA I7 8G)
451AFX31L18 (UMA I7 16G)
451AFX31L19 (DIS I7 16G QS)

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Schematic Document

(Omega Prime Comet Lake U)

Pilot

2019-07-15A

Rev: 1.0 (A00)

BOM Structure

PCB@ : PCB PN

UMA@ : No GPU SKU

DIS@ : GPU SKU

PRE_EVT@/EVT@/DVT1@/DVT2@/PILOT@ : Board ID

2G_G5@/N17H2G@/N17M2G@ : VRAM type

RTD3@ : TBT RTD3 Component

G3@ : EC G3 Sharing Mode

MAF@ : Master Attached Flash Sharing Mode

WWAN@ : WWAN Component

JEFF@ : Intel WLAN Jefferson Peak

TS@ : Touch Screen Component

FFS@ : Free Fall Sensor

XDP@ : XDP Component

DEBUG@ : Debug Component

CONN@ : Connector Component

@ : Un-pop Component

@RTD3@ : TBT RTD3 Un-POP Component

@WWAN@ : WWAN Un-POP Component

EMI@/ESD@/RF@ : EMI, ESD and RF Component

WWAN@RF@/WWAN@EMI@/WWAN@ESD@ : RF, EMI and ESD Component for WWAN

DISRF@ : RF Component for GPU

TS@RF@ : RF Component for Touch Screen

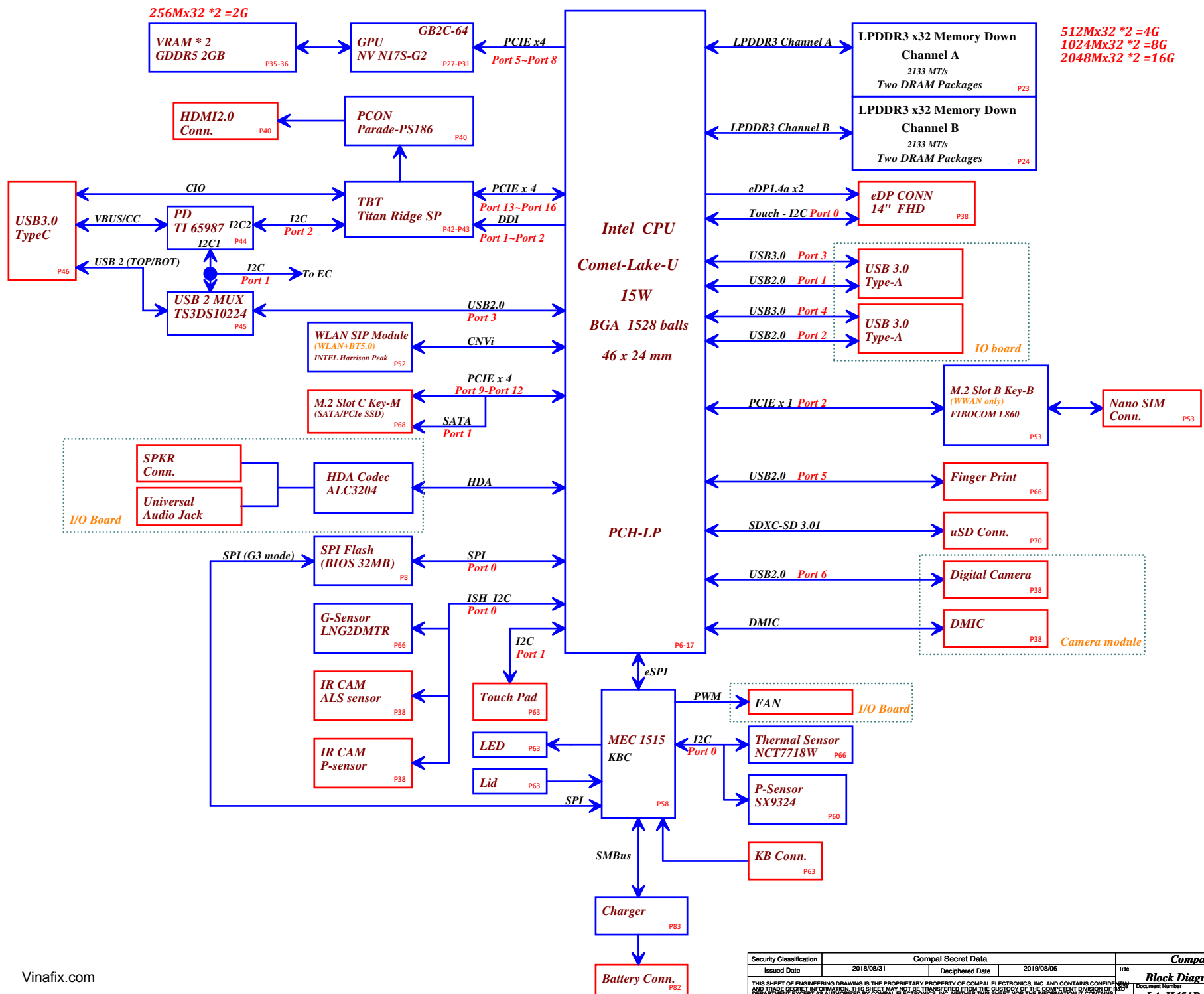
@EMI@/@ESD@/@RF@ : EMI, ESD and RF Un-POP Component

@WWAN@RF@/@WWAN@EMI@ : RF and EMI Un-POP Component for WWAN

S4G@/S8G@/S16G@/M4G@/M8G@/M16G@/S4G@/S8G@/S16G@ : LPDDR3 type

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Date: Monday, July 15, 2019			Rev 1.0
Sheet 1 of 100			



State	Signal	SLP S3#	SLP S4#	SLP S5#	ALWAYS PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0		HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM) / M3		LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M3		LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M3		LOW	LOW	LOW	ON	OFF	OFF	OFF
G3		OFF	OFF	OFF	OFF	OFF	OFF	OFF
DS3		---	---	---	---	---	---	---

Voltage Rails

Power Plane	Description	S0	S3	S4/S5
+TBTA_VBUS	Adapter power supply	N/A	N/A	N/A
+8.4V_BATT	Battery power supply	N/A	N/A	N/A
B+	AC or battery power rail for System	ON	ON	ON
+RTC_CELL	RTC power	ON	ON	ON
+3VALW_DSW	+3VALW power for PCH DSW rails	ON	ON	ON*
+5VALW	System +5V always on power rail	ON	ON	ON*
+3VALW	System +3V always on power rail	ON	ON	ON*
+1.8V_PRIM	System +1.8V always on power rail	ON	ON	ON*
+1.05V_PRIM	System +1.05V always on power rail	ON	ON	ON*
+1.2V_DDR	LPDDR3 +1.2V power rail	ON	ON	OFF
+1.8VU	LPDDR3 +1.8V power rail	ON	ON	OFF
+0.6V_DDR_VTT	DDR +0.6V power rail for DDR terminator	ON	OFF	OFF
+VCCST	+1.05 VCCST power rail	ON	ON	OFF
+VCCSTG	+1.05 VCCSTG power rail	ON	OFF	OFF
+VCCIO	+1.05 VCCIO power rail	ON	OFF	OFF
+VCC_CORE	Core voltage for CPU	ON	OFF	OFF
+VCC_GT	Sliced graphics power rail	ON	OFF	OFF
+VCC_SA	System Agent power rail	ON	OFF	OFF
+3VLP	+19VB to +3VLP power rail for suspend power	ON	ON	ON
+3VALW_PCH	+3VALW power for PCH suspend rails	ON	ON	ON*
+5VS	System +5VS power rail	ON	OFF	OFF
+3VS	System +3VS power rail	ON	OFF	OFF
+GPU_CORE	Core power rail for GPU	ON	OFF	OFF
+1.35VS_VRAM	+1.35V power rail for GPU	ON	OFF	OFF
+1.8VS_DGPU_AON	+3V power rail for GPU	ON	OFF	OFF
+1.8VS_DGPU_MAIN	+1.8V power rail for GPU	ON	OFF	OFF
+1.0VS_DGPU	+1.0V power rail for GPU	ON	OFF	OFF

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF

		Omega			
		X4EAFX31L01	X4EAFX31L02	X4EAFX31L03	X4EAFX31L04
X4E		SMT EMC EE DIS AH451 EDW40	SMT EMC EE UMA AH451 EDW40	SMT EMC EE DIS W/O WWAN AH451 EDW40	SMT EMC EE UMA W/O WWAN AH451 EDW40
EMI	EMI@	V	V	V	V
EMI for WWAN	WWAN@EMI@	V	V	V	V
ESD	ESD@	V	V	V	V
ESD for WWAN	WWAN@ESD@	V	V	V	V
RF	RF@	V	V	V	V
RF for GPU	DISRF@	V	V	V	V
RF for WWAN	WWAN@RF@	V	V	V	V
RF for Touch Screen	TS@RF@	V	V	V	V
EMI Reserve, un-pop	@EMI@				
EMI Reserve, un-pop	@WWAN@EMI@				
ESD Reserve, un-pop	@ESD@				
RF Reserve, un-pop	@RF@				
RF Reserve, un-pop	@WWAN@RF@				

USB 2.0	DESTINATION
1	USB2.0 Port1, IO/B
2	USB2.0 Port2, IO/B
3	USB2.0 MUX
4	NC
5	Finger printer
6	Camera
7	NC
8	NC
9	WWAN
10	NC

DDI	DESTINATION
Lane 1	TBT
Lane 2	TBT

USB3.0	PCIE	SATA	DESTINATION
USB3.0-1	PCIE-1		WWAN
USB3.0-2	PCIE-2		NC
USB3.0-3	PCIE-3		USB3.0 Port1, IO/B
USB3.0-4	PCIE-4		USB3.0 Port2, IO/B
USB3.0-5	PCIE-5		GPU
USB3.0-6	PCIE-6		GPU
	PCIE-7		GPU
	PCIE-8		GPU
	PCIE-9		NVME SSD
	PCIE-10		NVME SSD
	PCIE-11	SATA-0	NVME SSD
	PCIE-12	SATA-1A	NVME SSD
	PCIE-13		TBT
	PCIE-14		TBT
	PCIE-15	SATA-1B	TBT
	PCIE-16	SATA-2	TBT

CLK_PCIE	CLK_REQ	DESTINATION
0	0	GPU
1	1	None
2	2	WWAN
3	3	TBT
4	4	SSD
5	5	None

Refer Page 58

Board ID & Model ID Table

#	Pull-down	Pull-up	Voltage	Board ID	Model ID
1	100K	10K	3.000	Pre-EVT	UMA
2	100K	17.8K	2.801	EVT	DIS
3	100K	27K	2.598		
4	100K	37.4K	2.402	DVT1	
5	100K	49.9K	2.201	DVT2	
6	100K	64.9K	2.001		
7	100K	82.5K	1.808	Pilot	
8	100K	107K	1.594		
9	100K	154K	1.299		
10	100K	200K	1.100		

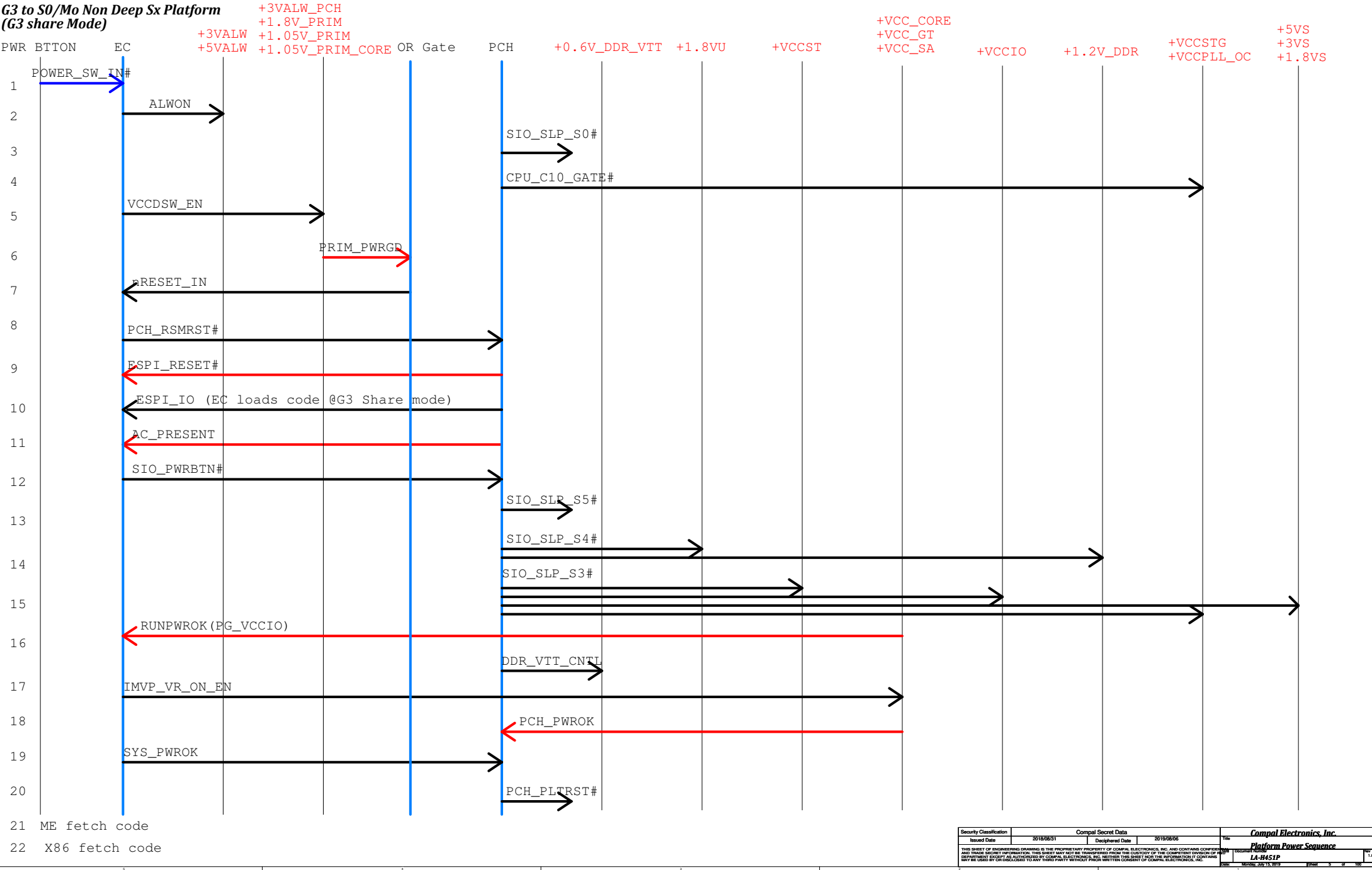
Figure 6-1. High Speed I/O (HSIO) Lane Multiplexing in CNL U PCH-LP

Flex I/O Lane	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
High Speed I/O (HSIO) Type and Lane	USB3.1 Gen1/Gen2 x1	USB3.1 Gen1/Gen2 x2	USB3.1 Gen1/Gen2 x3	USB3.1 Gen1/Gen2 x4	USB3.1 Gen1/Gen2 x5	PCIE# #7	PCIE# #8	PCIE# #9	PCIE# #10	PCIE# #11	PCIE# #12	PCIE# #13	PCIE# #14	PCIE# #15	PCIE# #16	PCIE# #17
Intel® RST Support	No Support	No Support	No Support	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes

		431AFX31L05	431AFX31L02	431AFX31L06	431AFX31L07	431AFX31L09	431AFX31L08	431AFX31L15	431AFX31L11	431AFX31L17	431AFX31L12	431AFX31L14
X43		SMT MB AH451 EDW40 CML DIS I5 8G	SMT MB AH451 EDW40 CML DIS I5 8G N	SMT MB AH451 EDW40 CML DIS I5 8G WWAN	SMT MB AH451 EDW40 CML DIS I5 16G	SMT MB AH451 EDW40 CML DIS I7 16G	SMT MB AH451 EDW40 CML DIS I7 16G N	SMT MB AH451 EDW40 CML UMA I5 8G WWAN	SMT MB AH451 EDW40 CML UMA I5 8G WWAN N	SMT MB AH451 EDW40 CML UMA I7 8G	SMT MB AH451 EDW40 CML UMA I7 8G N	SMT MB AH451 EDW40 CML UMA I5 8G
PCB PN	PCB@	V	V	V	V	V	V	V	V	V	V	V
CPU V0 I5-QRY2	WHL_I5_V0@											
CPU V0 I7-QRYX	WHL_I7_V0@											
CPU Q5 I5-QS8G	CML_I5_OS@											
CPU Q5 I7-QS8F	CML_I7_OS@											
CPU MP I5-SR8KY	CML_I5_MP@	V	V	V	V	V	V	V	V	V	V	V
CPU MP I7-SR8KW	CML_I7_MP@											
WHL only	WHL@											
GPU ID	UMA@											
DIS@	DIS@	V	V	V	V	V	V	V	V	V	V	V
PRE EVT@	PRE EVT@											
EVT@	EVT@											
DVT1@	DVT1@											
DVT1.1@	DVT1.1@											
DVT2@	DVT2@											
PILOT@	PILOT@	V	V	V	V	V	V	V	V	V	V	V
2G_G5@	2G_G5@	V	V	V	V	V	V	V	V	V	V	V
Thunderbolt RTD3	RTD3@	V	V	V	V	V	V	V	V	V	V	V
EC G3 Sharing Mode	G3@	V	V	V	V	V	V	V	V	V	V	V
SPI MAF Mode	MAF@											
WWAN/NON-WWAN	WWAN@											
NONWWAN@	NONWWAN@	V	V	V	V	V	V	V	V	V	V	V
WLAN Jefferson	JEFF@											
Peak/Harrison Peak	HARSN@	V	V	V	V	V	V	V	V	V	V	V
Touch Screen	TS@	V	V	V	V	V	V	V	V	V	V	V
XDP debug	XDP@	V	V	V	V	V	V	V	V	V	V	V
On board switch	CHSUG@											
MDVC@	MDVC@											
GD@	GD@	V	V	V	V	V	V	V	V	V	V	V
WB@	WB@											
Connector	CONN@											
EMI/ESD/RF	X4E	X4EAFX31L03	X4EAFX31L03	X4EAFX31L01	X4EAFX31L01	X4EAFX31L03	X4EAFX31L03	X4EAFX31L02	X4EAFX31L02	X4EAFX31L04	X4EAFX31L04	X4EAFX31L04
LPDDR3 Option	X76	X7681431L07	X7681431L07	X7681431L07	X7681431L07	X7681431L10	X7681431L10	X7681431L07	X7681431L07	X7681431L07	X7681431L07	X7681431L07
		X7681431L08	X7681431L08	X7681431L08	X7681431L08	X7681431L11	X7681431L11	X7681431L08	X7681431L08	X7681431L08	X7681431L08	X7681431L08
VRAM Option	X76	X7681431L01	X7681431L01	X7681431L01	X7681431L01	X7681431L01	X7681431L01	X7681431L08	X7681431L08	X7681431L08	X7681431L08	X7681431L08
		X7681431L02	X7681431L02	X7681431L02	X7681431L02	X7681431L02	X7681431L02					
Reserved, un-pop	@											
Reserved, un-pop	@RTD3@											
Reserved, un-pop	@WWAN@											
Reserved, un-pop	@TS@											

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					LA-H451P
				Date	Monday, July 15, 2019
				Sheet	3 of 100

G3 to S0/Mo Non Deep Sx Platform
(G3 share Mode)



[illegible]

Main Func = SOC

COMPENSATION FOR EDP_COMP
CAD note:
Trace width=5 mils, Spacing=25mils
Max length=600mils

COMPENSATION FOR OPIRCOMP
CAD Note:
Min trace width=10 mils, Max trace length=500 mils

COMPENSATION FOR OPIRCOMP
CAD Note:
Min trace width=10 mils, Max trace length=500 mils

WHL-U42_BGA1528

LA-H451P

Security Classification
Compal Secret Data

Issued Date
2018/08/31

Deciphered Date
2019/08/06

Title
WHL-U(1/12)DDI,MSIC,XDP,EDP

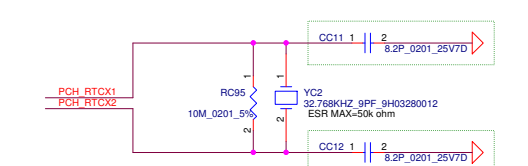
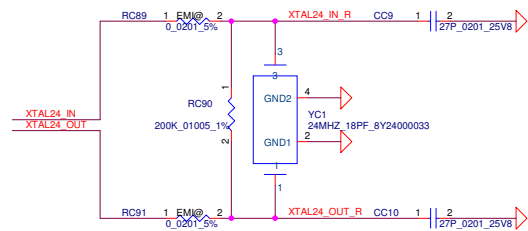
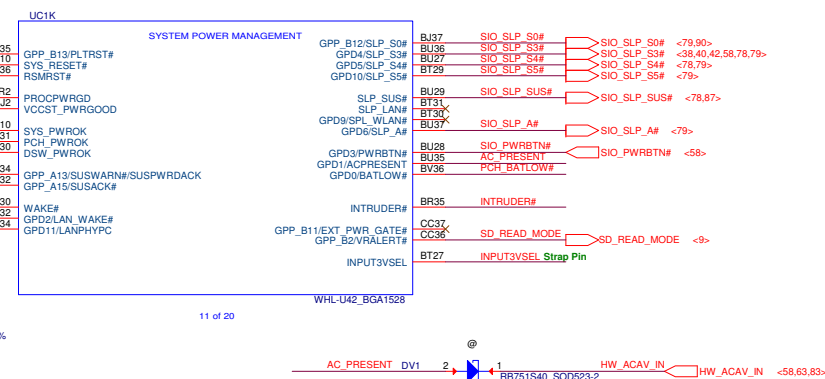
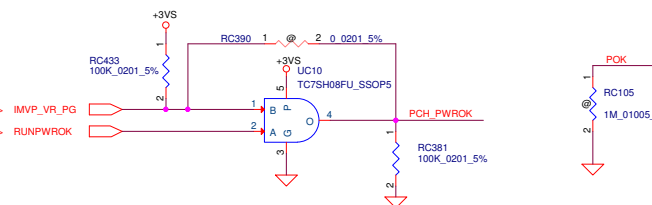
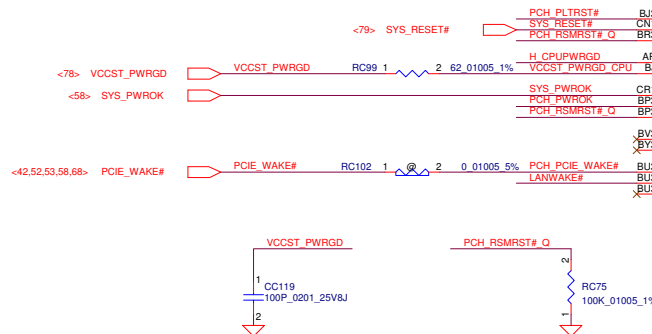
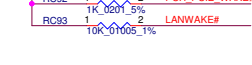
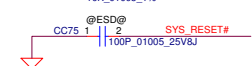
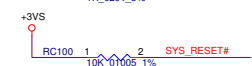
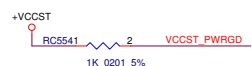
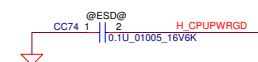
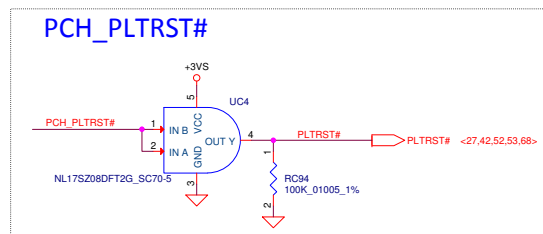
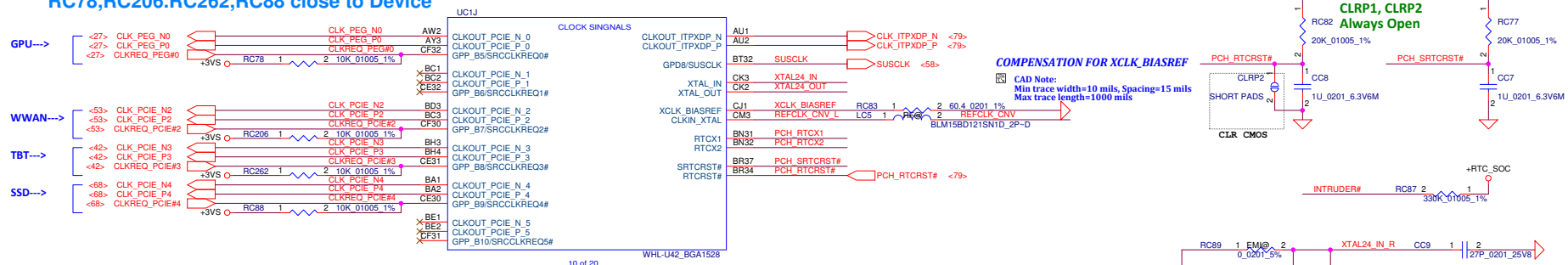
Document Number
LA-H451P

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1.0

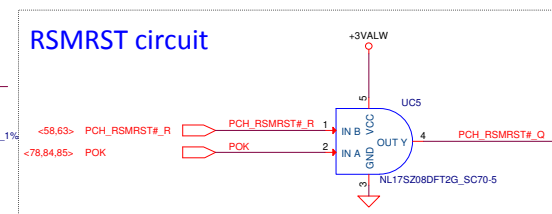
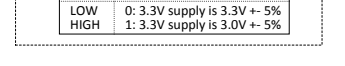
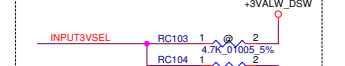
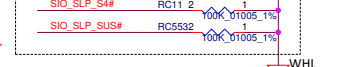
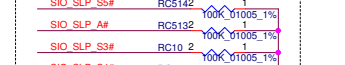
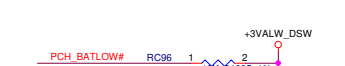
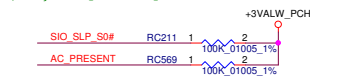
Date
Monday, July 15, 2019

Sheet
6 of 100

RC78,RC206,RC262,RC88 close to Device

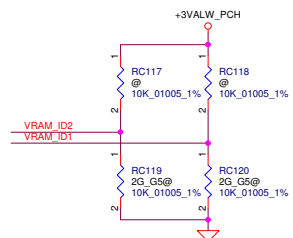
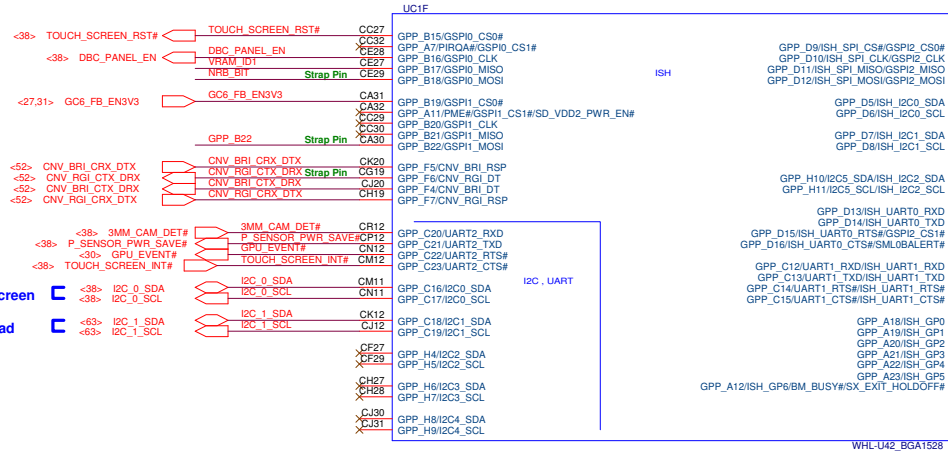
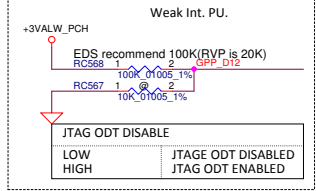
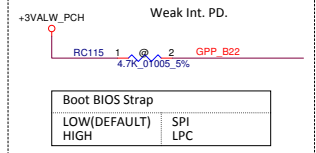
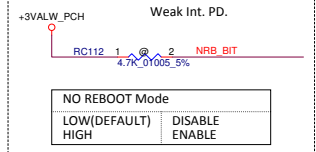
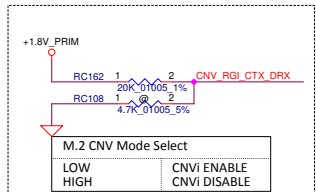
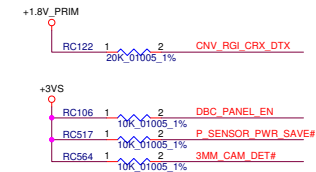


DVT1
Change CC11, CC12 from 10P_0201 to 8.2P_0201.

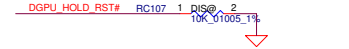
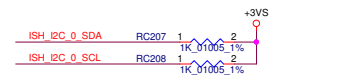


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				LA-H451P	
Date:	Monday, July 15, 2019	Sheet	10	of	100

Main Func = SOC



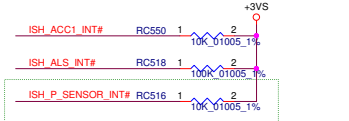
VRAM ID (PCBA VRAM Size Config.)	VBIOS_ID2 (GPP_CN23)	VBIOS_ID1 (GPP_CE27)
2G GDDR5	0	0
Reserved	0	1
Reserved	1	0
Reserved	1	1



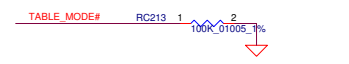
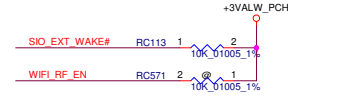
IR CAM ALS / IR CAM P-sensor / G-sensor (3.3V)

SAR P-sensor (1.8V) (reserved)

pull up on device side



DVT 1.0
Change net "ISH_P_SENSOR_INT#" connect from GPP_A6 to GPP_A19/ISH_GP1.
Move RC516 from page0 to page11.



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2019/08/06				Title				WHL-U(6/12)GPIO			
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Date:				Monday, July 15, 2019				Sheet 11 of 100			
Rev 1.0											

Main Func = SOC

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GPU ---->

PCIE SSD---->

TBT ---->



COMPENSATION FOR PCIE_RCOMP

CAD Note:
Min trace width=10 mils
Max trace mismatch=5 mils

CR28
CP28
CN28
CM28

UC1H

PCIE / USB3.1 / SATA

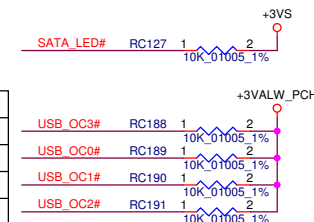
USB2.0



COMPENSATION FOR USB2_COMP

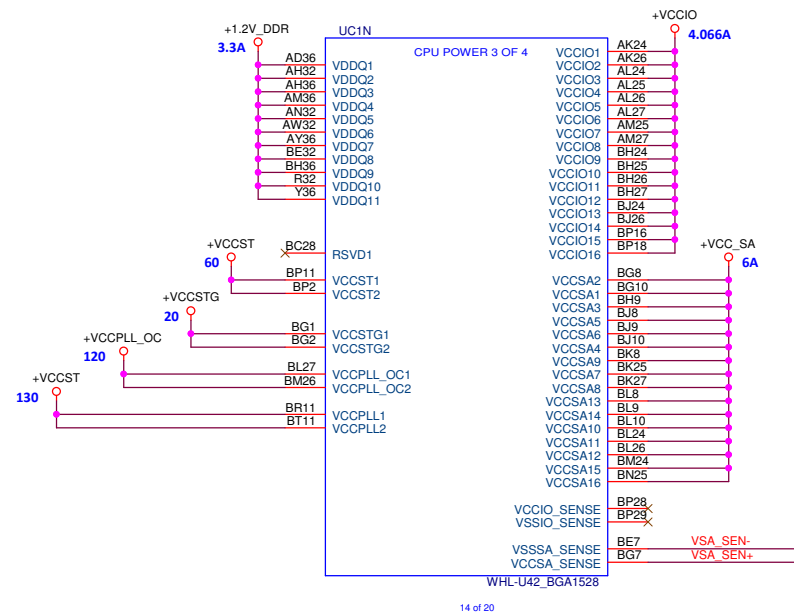
CAD Note:
Min trace width=50 Ohm, Spacing=15 mils
Max trace length=500 mils

GPIO	DEVICE CONTROL
USB_OC0#	USB Port (DB)
USB_OC1#	NA
USB_OC2#	NA
USB_OC3#	NA
DEVSLP0	NA
DEVSLP1	M.2 SSD
DEVSLP2	NA

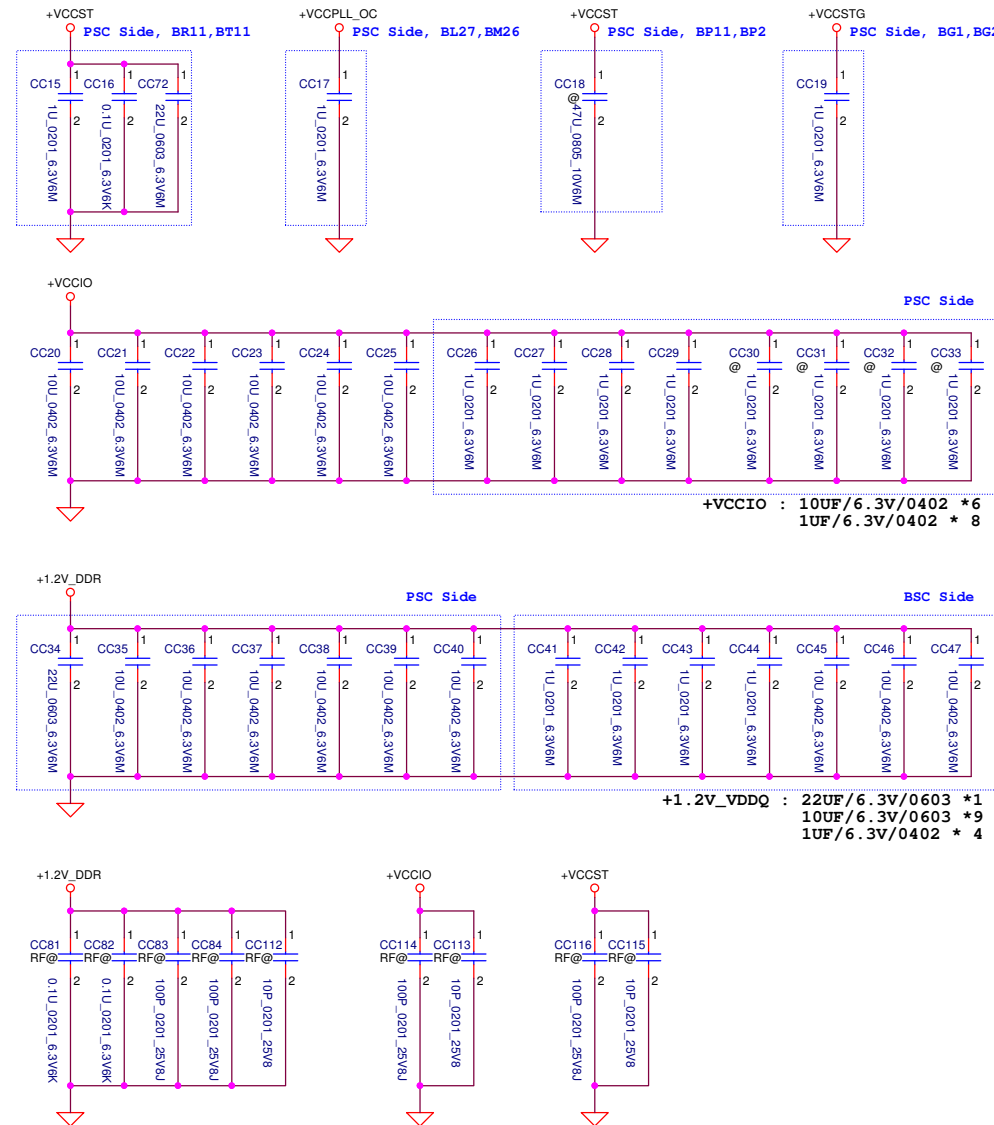
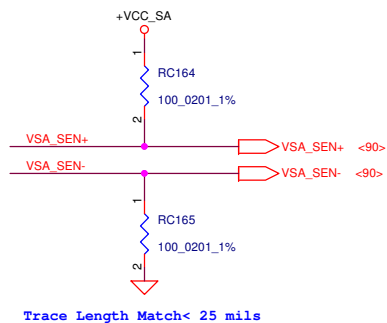


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						Document Number		Rev	
						LA-H451P		1.0	
						Date: Monday, July 15, 2019		Sheet 12 of 100	

Main Func = SOC

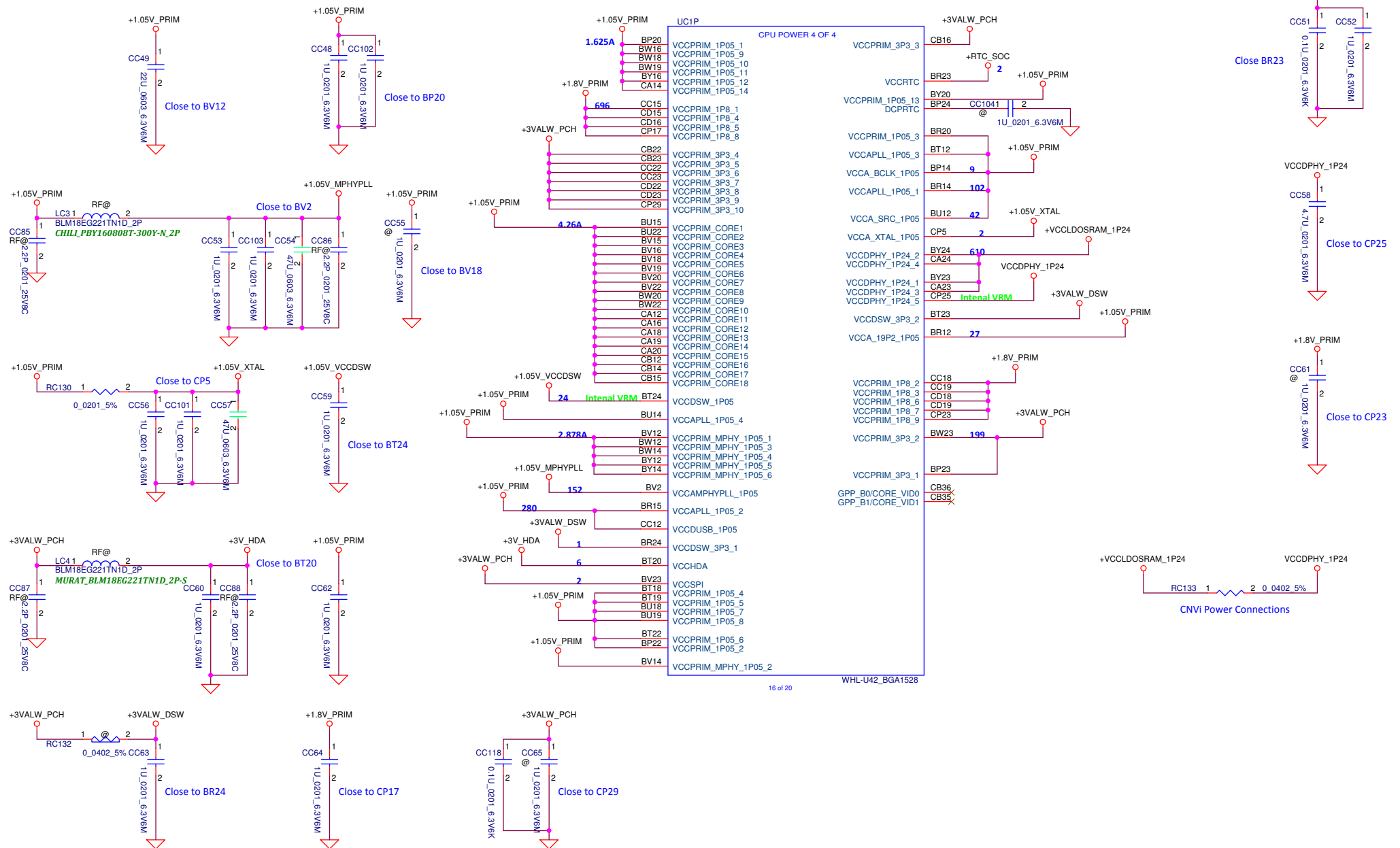


14 of 20



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				Date	Monday, July 15, 2019
				Sheet	13 of 100

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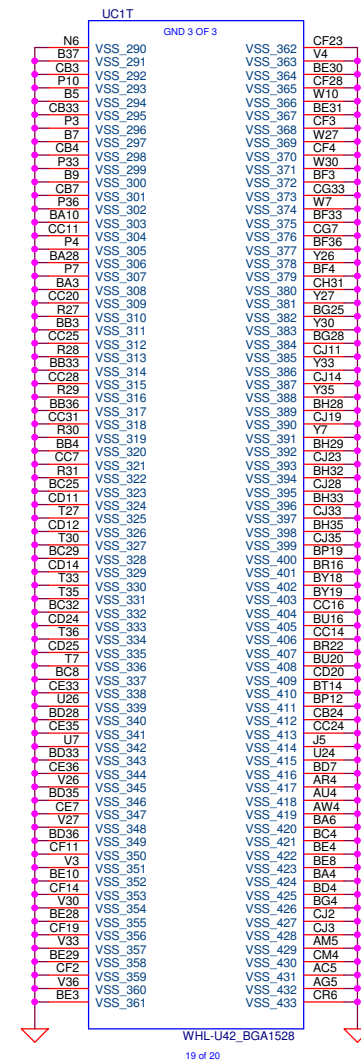
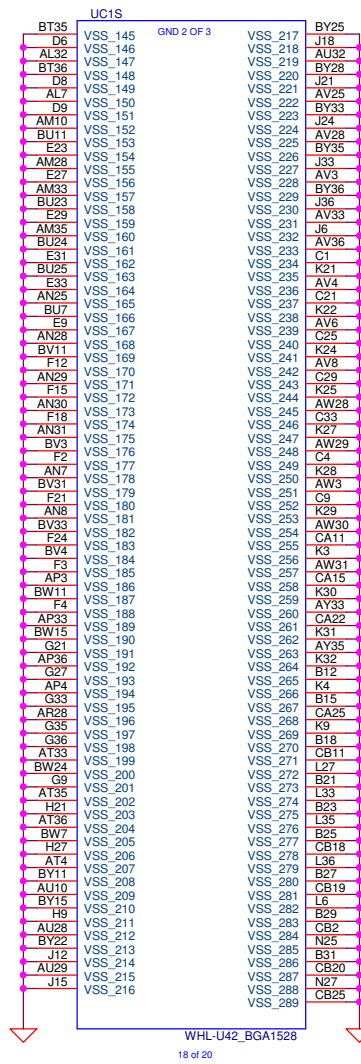
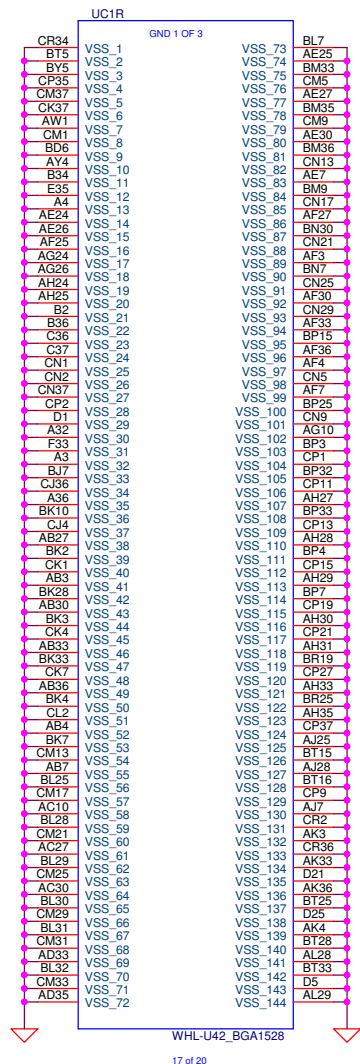


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				LA-H451P	1.0	
				Date: Monday, July 15, 2019	Sheet	14 of 100

1

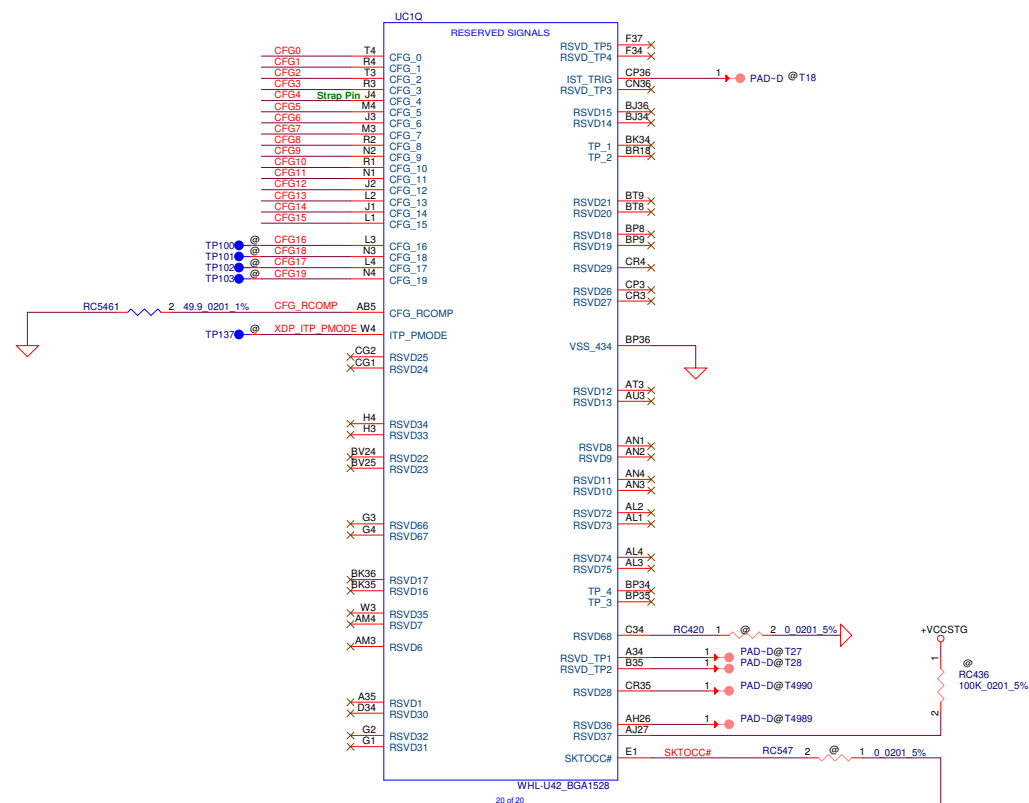
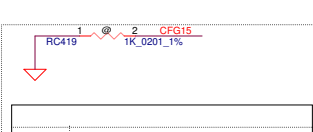
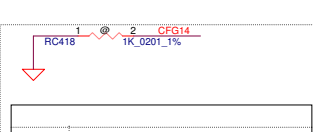
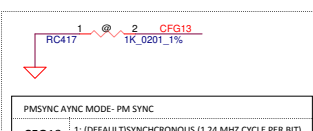
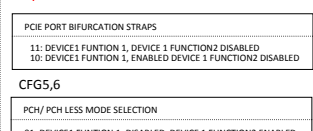
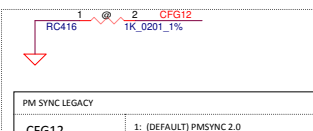
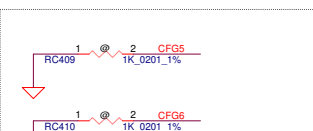
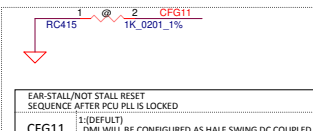
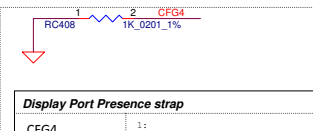
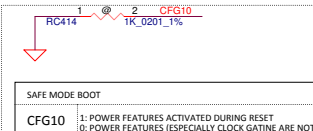
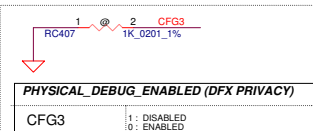
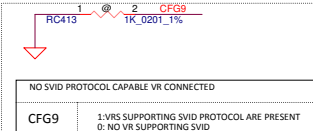
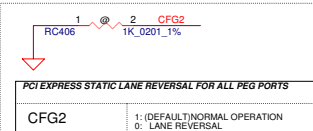
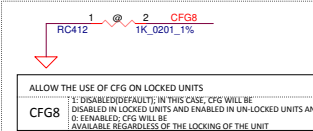
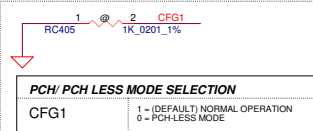
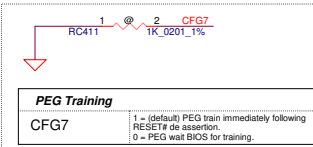
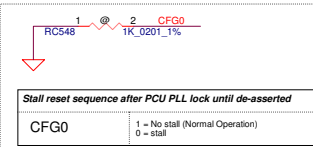
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				Date	Monday, July 15, 2019
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Date:				Monday	July 15, 2019
				Sheet	17 of 100

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				Sheet	20	of 100

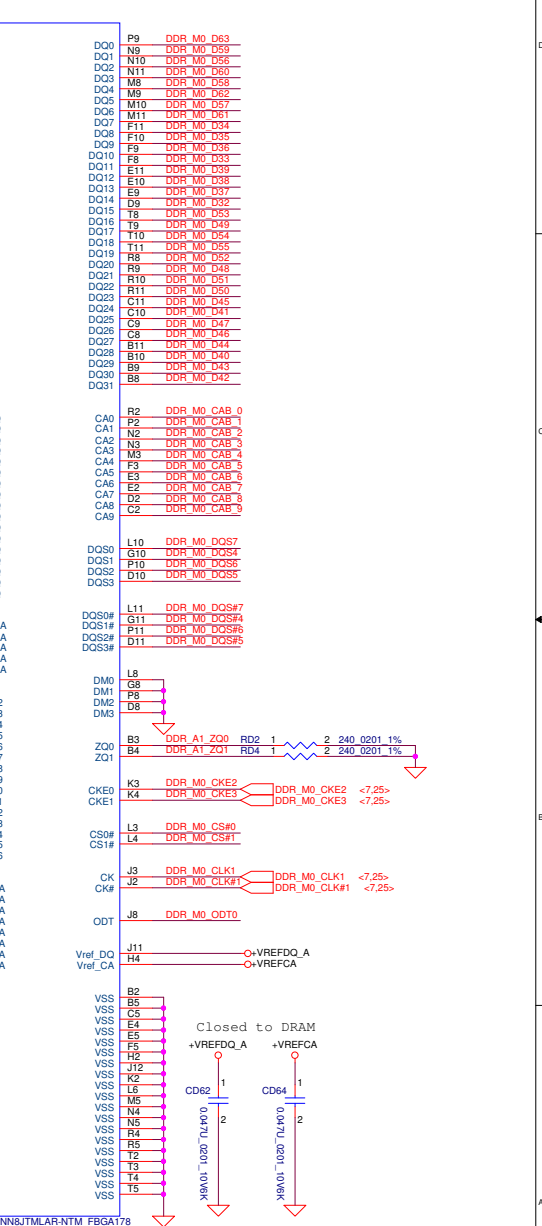
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				Sheet	21	of 100

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				Sheet	22	of 100

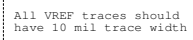
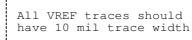
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H9CCNNCLGALAR-NVD_FBGA178



All VREF traces should
have 10 mil trace width

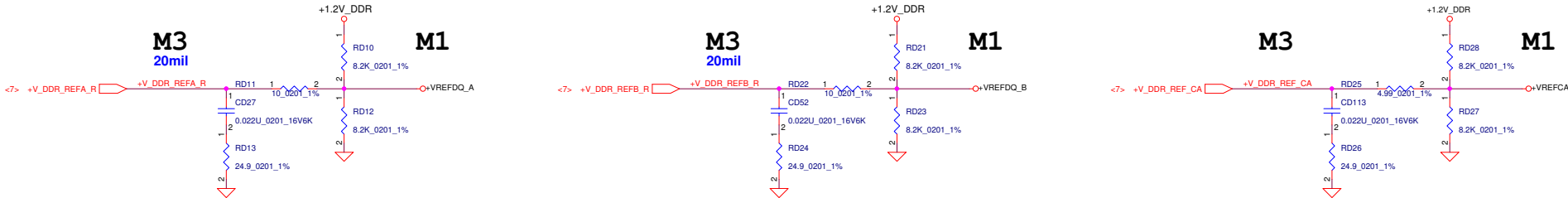
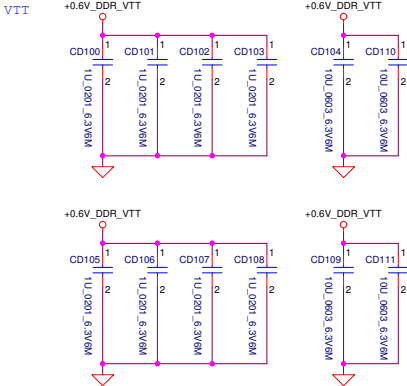
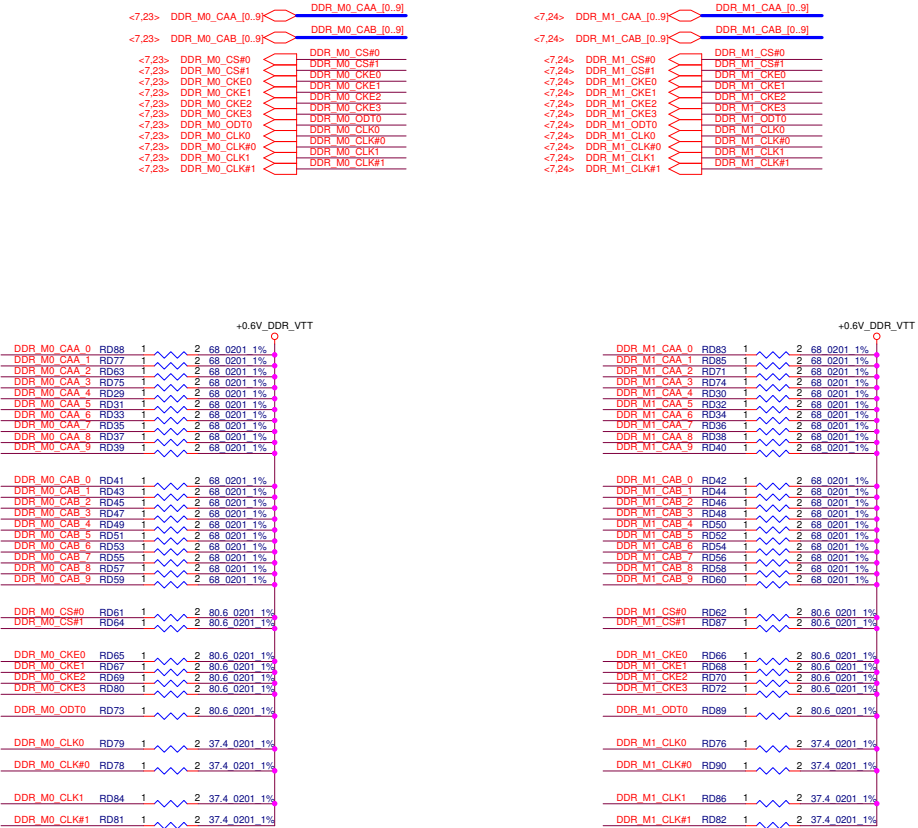
Rev	
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Date: Monday, July 15, 2019			Sheet	24 of 100

Main Func = DDR



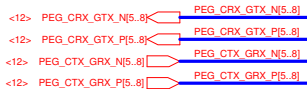
VREF traces should be at least 20 mils wide with 20 mils spacing to other signals/planes.

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				Sheet	26	of 100

Main Func = GPU

PCIE X4 Bus



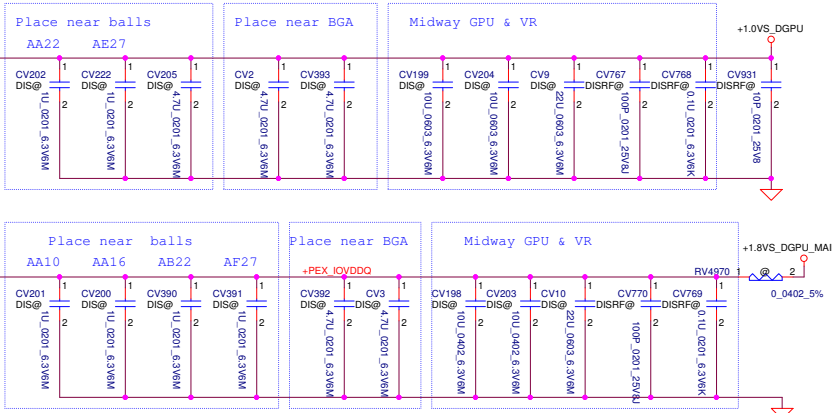
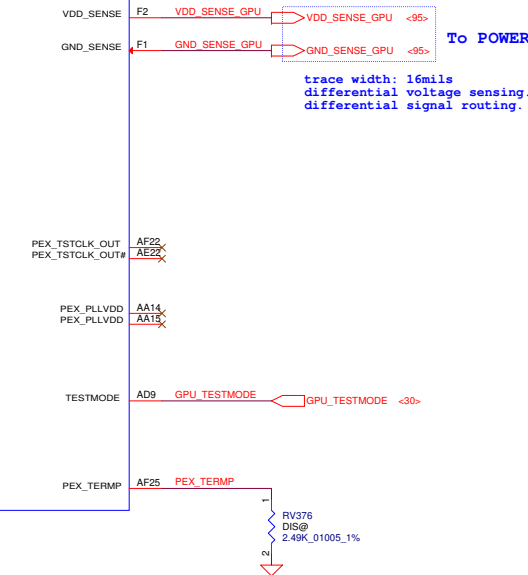
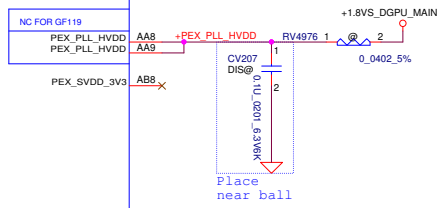
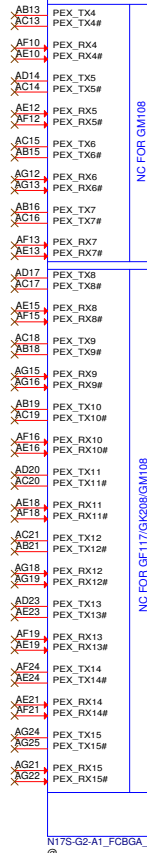
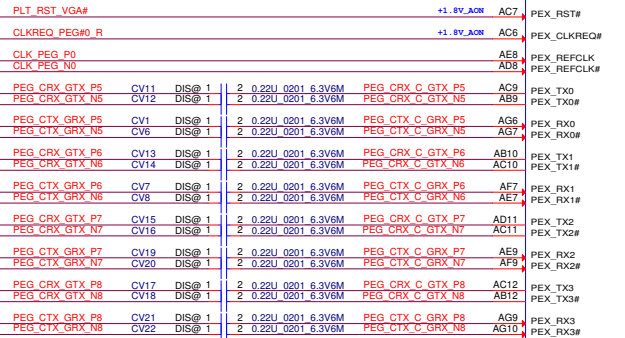
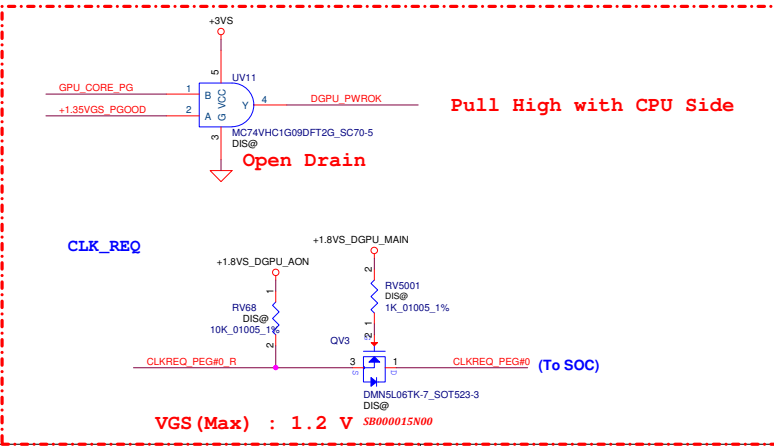
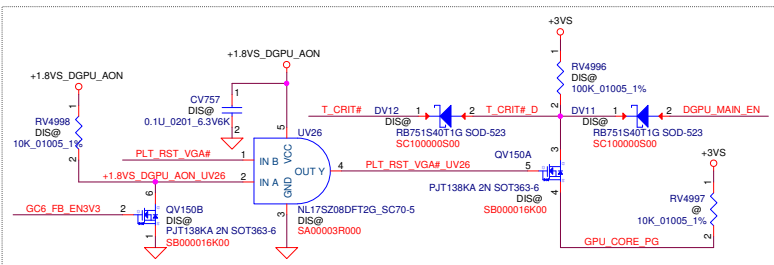
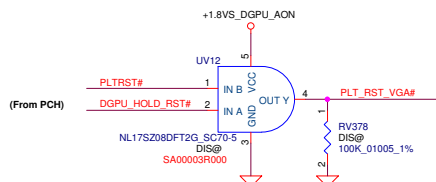
PCIE CLK



GPIO
Pull High with CPU Side

Reset Control

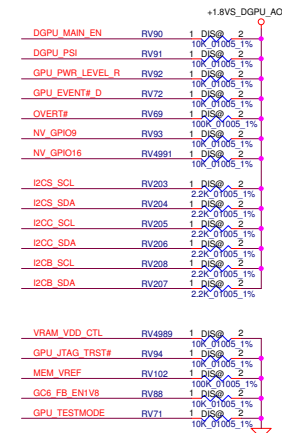
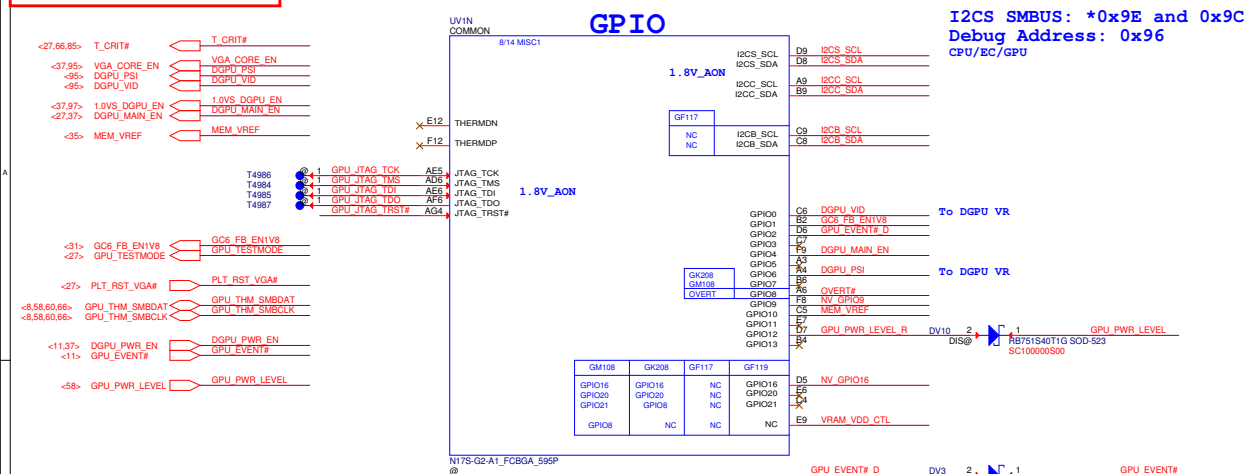
1.8V AND GATE



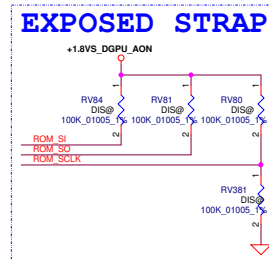
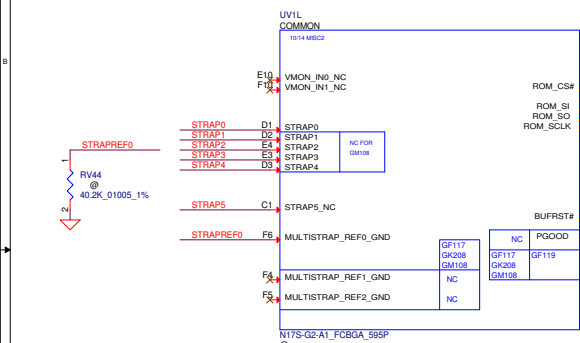
Rail (GPU Ball) Name	Balls	Voltage; Current	Filtering under GPU	Filtering Near GPU
PEX_DVDD	6	1.0V	2 X 1uF (0402 X5R)	1Hear GPU: 2 X 4.7uF (0603) Midway btw GPU & VR: 2 X 10uF (0805) 1 X 22uF (0805)

Rail (GPU Ball) Name	Balls	Voltage; Current	Filtering under GPU	Filtering Near GPU
PEX_HVDD	14	1.8V	4 X 1uF (0402 X5R)	1Hear GPU: 2 X 4.7uF (0603) Midway btw GPU & VR: 2 X 10uF (0805) 1 X 22uF (0805)
PEX_PLL_HVDD	2	1.8V	1 X 0.1uF (0402)	

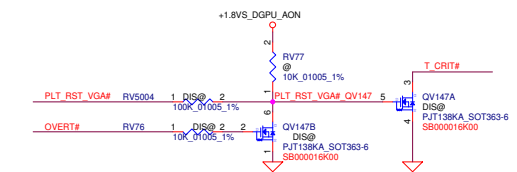
Main Func = GPU



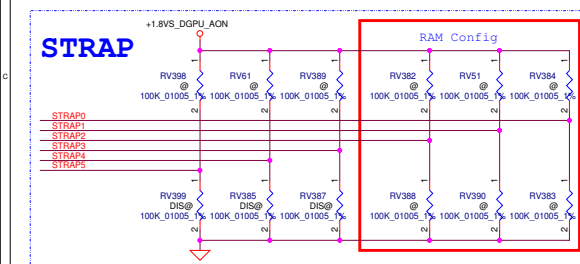
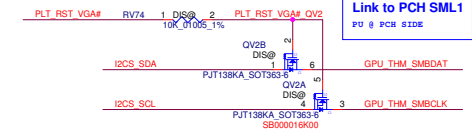
GPIO Number	GPIO Name	I/O	Functional Description	I/O Termination
GPIO0	HVDD0_PWM	O	PWM Output to control HVDD0	0 to 1V8 PWM output
GPIO1	GC6M: GC6_FB_EH	O	FB Enable for GC6 2.1	Open Drain 10 kΩ pull-down to 1V8_AOH, unless driven actively.
GPIO2	GC6M: GPU_EVENT*/WAKE*	I	GPU wake signal for GC6 2.1	Open Source 10 kΩ pull-up to 1V8_AOH
GPIO3	HVDDDS_PWM	I/O	PWM output to control the HVDDDS power supply	Open Drain 10 kΩ pull-up to 1V8_AOH
GPIO4	GC6M:1V8_MAIN_EN	O	GPU power sequencing for GC6 2.1	Open Drain 10 kΩ pull-up to 1V8_AOH
GPIO5	FRM_LCK*	I	Active low Frame Lock	Open Drain 10 kΩ pull-up to 1V8_AOH
GPIO6	HVDD0_PSI*/HVDDDS_PSI*	O	Phase Shedding (see Section 14.3.3)	10 kΩ pull-up to 1V8_AOH to enable multiple phases
GPIO7	LCD_BL_PWM	O	Panel Backlight enable	100 kΩ pull-down
GPIO8	MEM_VDD0_CTL	O	Memory voltage-control	Pull-up/pull-down to set the FBVDD/Q power-on voltage
GPIO9	THERM_ALERT*	I/O	Active Low Thermal Alert	Open Drain 10 kΩ pull-up to 1V8_AOH
GPIO10	MEM_VREF_CTL	O	Memory VREF Control	100 kΩ pull-down
GPIO11	LCD_VREF* Quadro-Eye_Brake*	O	Panel Power enable	100 kΩ pull-down
GPIO12	PWR_LEVEL	I	AC power detect or power supply overdraw input	100 kΩ pull-up to 1V8_AOH
GPIO13	LCD_BLEN	O	LCD Panel Backlight Enable	Panel Backlight Enable
GPIO14	HPD_IFPA*	I	Hot Plug Detect for IFPA	Inverted Input. See Figure 14.5
GPIO15	HPD_IFPB*	I	Hot Plug Detect for IFPB	Inverted Input. See Figure 14.5
GPIO16	GC6M: SYS_PEX_RST_MON*	I	System side PCIe reset monitor	10 kΩ pull-up to 1V8_AOH unless driven actively
GPIO17	UNUSED	I/O		
GPIO18	UNUSED	I/O		
GPIO19	3D Vision	O	3D Vision L/R Signal	100 kΩ pull-down
GPIO21	MEM_VDD0_CTL	O	Frame Buffer VDD select	Open Drain; Pull-up/pull-down to set the FBVDD/Q power-on voltage at boot up
GPIO22	UNUSED	I/O		
GPIO23	GC6M: GPU_PEX_RST_HOLD*	O	GPU PCIe self-reset control	Open Drain 10 kΩ pull-up to 1V8_AOH



Row Index	Strap Pins <small>see Note</small>			Resulting SORx_EXPOSED Enablements			
	ROM_S0	ROM_S1	ROM_SCLK	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
15	L	L	L	ENABLED	ENABLED	ENABLED	ENABLED
14	L	L	H	ENABLED	ENABLED	ENABLED	disabled
13	L	H	L	ENABLED	ENABLED	disabled	ENABLED
12	L	H	H	ENABLED	ENABLED	disabled	disabled
8	H	H	H	ENABLED	disabled	disabled	disabled
0	H	H	M	disabled	disabled	disabled	disabled
	M	X	X	(Reserved; do not configure)			
	All other Strap Configurations			(Reserved)			



Internal Thermal Sensor



Strap Pins see Note			RAMCFG Setting Number
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
L	L	L	0 (0x0000)
L	L	H	1 (0x0001)
L	H	L	2 (0x0002)
L	H	H	3 (0x0003)
H	L	L	4 (0x0004)
H	L	H	5 (0x0005)
H	H	L	6 (0x0006)
H	H	H	7 (0x0007)
L	L	M	8 (0x0008)
L	M	L	9 (0x0009)
L	M	H	10 (0x000A)
L	H	M	11 (0x000B)
M	L	L	12 (0x000C)
M	L	H	13 (0x000D)

Table 5.6 SMB ALT_ADDR, DEVID_SEL, PCIE_CFG, VGA_DEVICE

Strap Pins			Functions Selected by This Strapping			
STRAP5	STRAP4	STRAP3	SMG_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVID
L	L	L	0	0	0	0
L	L	H	0	0	0	1
L	H	L	0	0	1	0
L	H	H	0	0	1	1
H	L	L	0	1	0	0
H	L	H	0	1	0	1
H	H	L	0	1	1	0
H	H	H	0	1	1	1

SMB_ALT_ADDR	
Low	Single GPU
High	Dual GPU







DEVID_SEL	
Low	Original Device ID
High	Re-brand Device ID

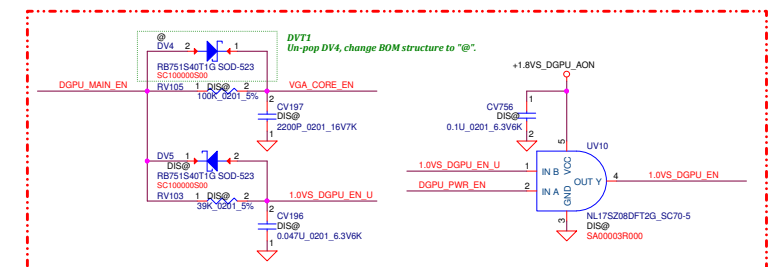
VGA_DEVICE	
Low	3D Device
High	VGA Device

PCIE_CFG	
Low	Normal signal swing
High	Reduce the signal amplitude

Table 5. N175-G0/G2 GDDR5 Recommended Memories

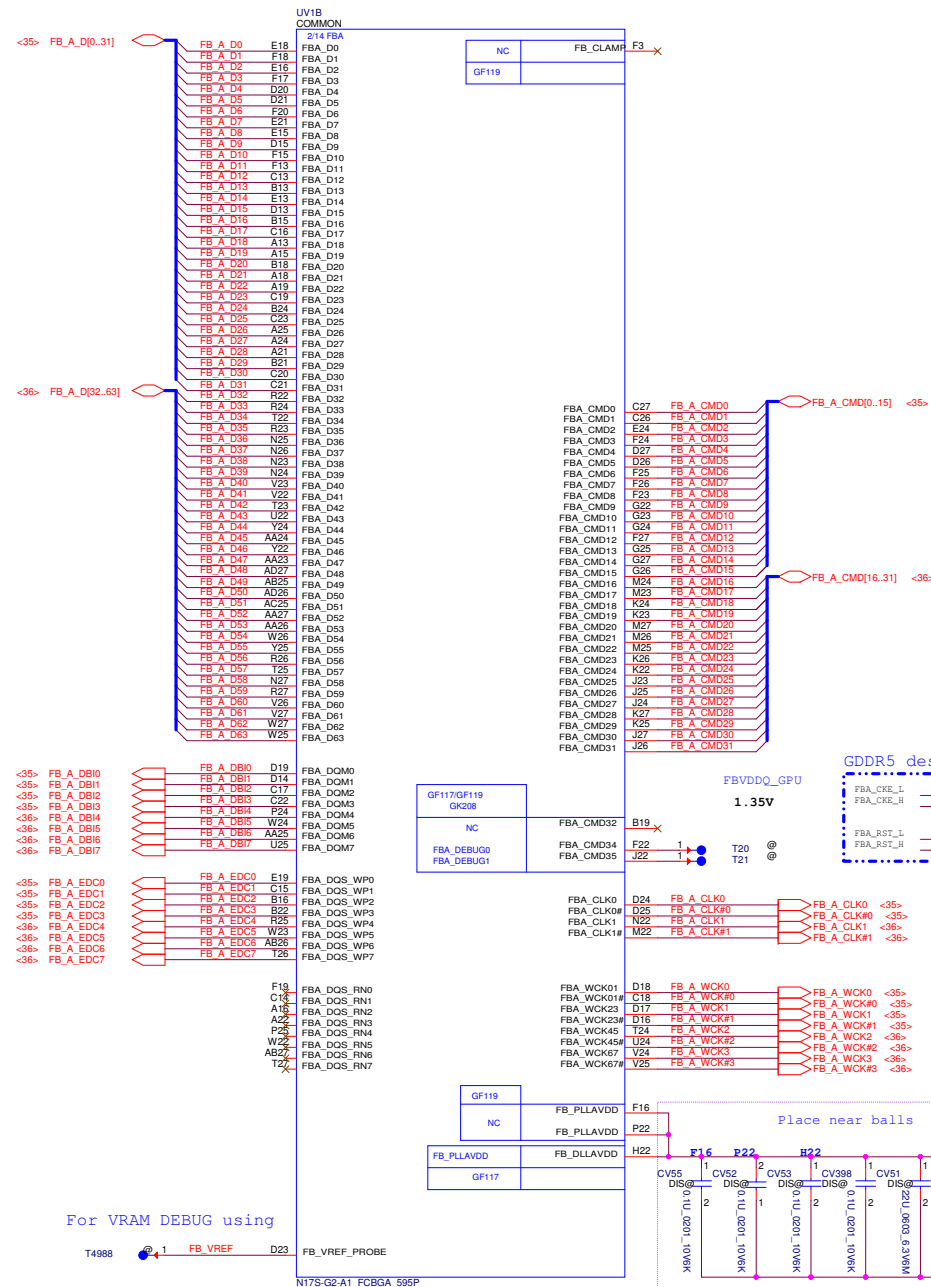
Memory Density	Allowed Memory Configuration	FBVD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code	Qual Plan	Status
8 Gb	256Mx32 512Mx16	1.35V	Micron	MTS1J256M32HF-80:B	B-11e	0x9	8 Gbps	N/A	Full	Production ready
			Hynix	H5GC8HJ4RJR-R2C	A-die	0xA	8 Gbps	N/A	Full	Production

RAM_CFG	STRAP2	STRAP1	STRAP0
0x09 (LML) M2G	 RV388 N17M2G	 RV390 N17M2G	 RV51 N17M2G
0x0A (LMH) H2G	 RV388 N17H2G	 RV390 N17H2G	 RV51 N17H2G



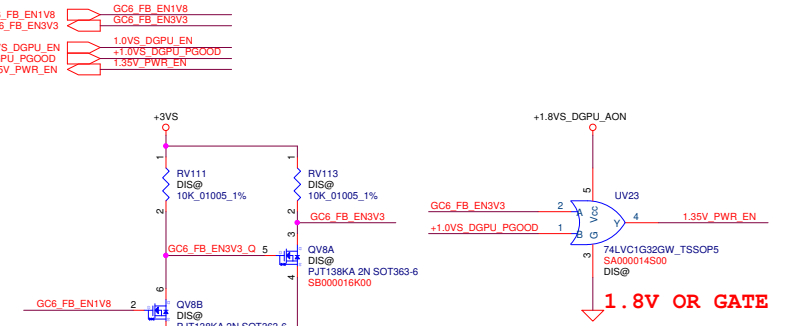
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Issued Date	2018/08/31	Deciphered Date	2019/08/06	Title	NV(4/5)-GPIO/Strap
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For GC6



GDDR5_BGA170_MIRR COMMAND MAP

	0_31	32_63
CMD0	CS*	
CMD1	A3_BA3	
CMD2	A2_BA0	
CMD3	A4_BA2	
CMD4	A5_BA1	
CMD5	WE*	
CMD6	A7_A8	
CMD7	A6_A11	
CMD8	ABI*	
CMD9	A12_RFU	
CMD10	A0_A10	
CMD11	Al_A9	
CMD12	RAS*	
CMD13	RST*	
CMD14	CKE*	
CMD15	CAS*	
CMD16		CS*
CMD17		A3_BA3
CMD18		A2_BA0
CMD19		A4_BA2
CMD20		A5_BA1
CMD21		WE*
CMD22		A7_A8
CMD23		A6_A11
CMD24		ABI*
CMD25		A12_RFU
CMD26		A0_A10
CMD27		Al_A9
CMD28		RAS*
CMD29		RST*
CMD30		CKE*
CMD31		CAS*



From DG-07158-001_v05_secured(NVIDIA Spec)

7.1.8 CKE* Signal

Two copies of the clock enable signal (CKE*) are provided for each memory partition of the GPU (Figure 7-4). These are connected to two DRAM components in the standard mode as point-to-point connections. The two signals are shared in the clamshell mode that will have four DRAM components (Figure 7-5). The CKE* signal requires a 10 kΩ pull-up resistor. This pull-up placement is not critical. The ODT is not provided for these signals.

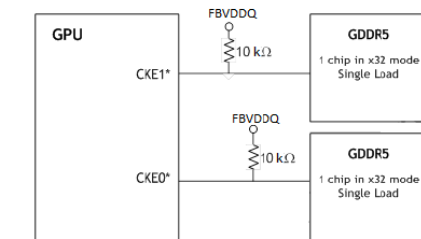


Figure 7-4. Clock Enable (CKE*) Signal Connection, x32 Mode

7.1.7.3 RST* Signal

Each channel (32-bit interface) of the GPU provides a single reset signal (Figure 7-3). This is connected to one DRAM component in the standard mode and two DRAM components in the clamshell mode. This signal requires one 10k Ω pull-down resistor in standard mode or in clamshell mode. The placement of this pull-down resistor should be at the end of the daisy-chain of this trace. The ODT is not provided for this signal.

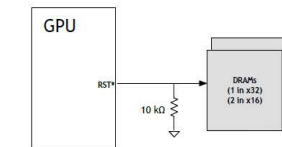


Figure 7-3. Reset Signal Connection

Rail (GPU Ball) Name	Balls	Voltage; Current	Filtering under GPU	Filtering Near GPU
FBA_PLL_AVDD	1	1.8V	2 X 0.1uF (0402 X7R)	1 X 300 bead (0603 max ESR 10 mΩ) 1 X 22uF (0805)
FBB_PLL_AVDD	1			
FB_REFPLL_AVDD	1	1.8V	0.1uF (0402 X5R)	

Reserve

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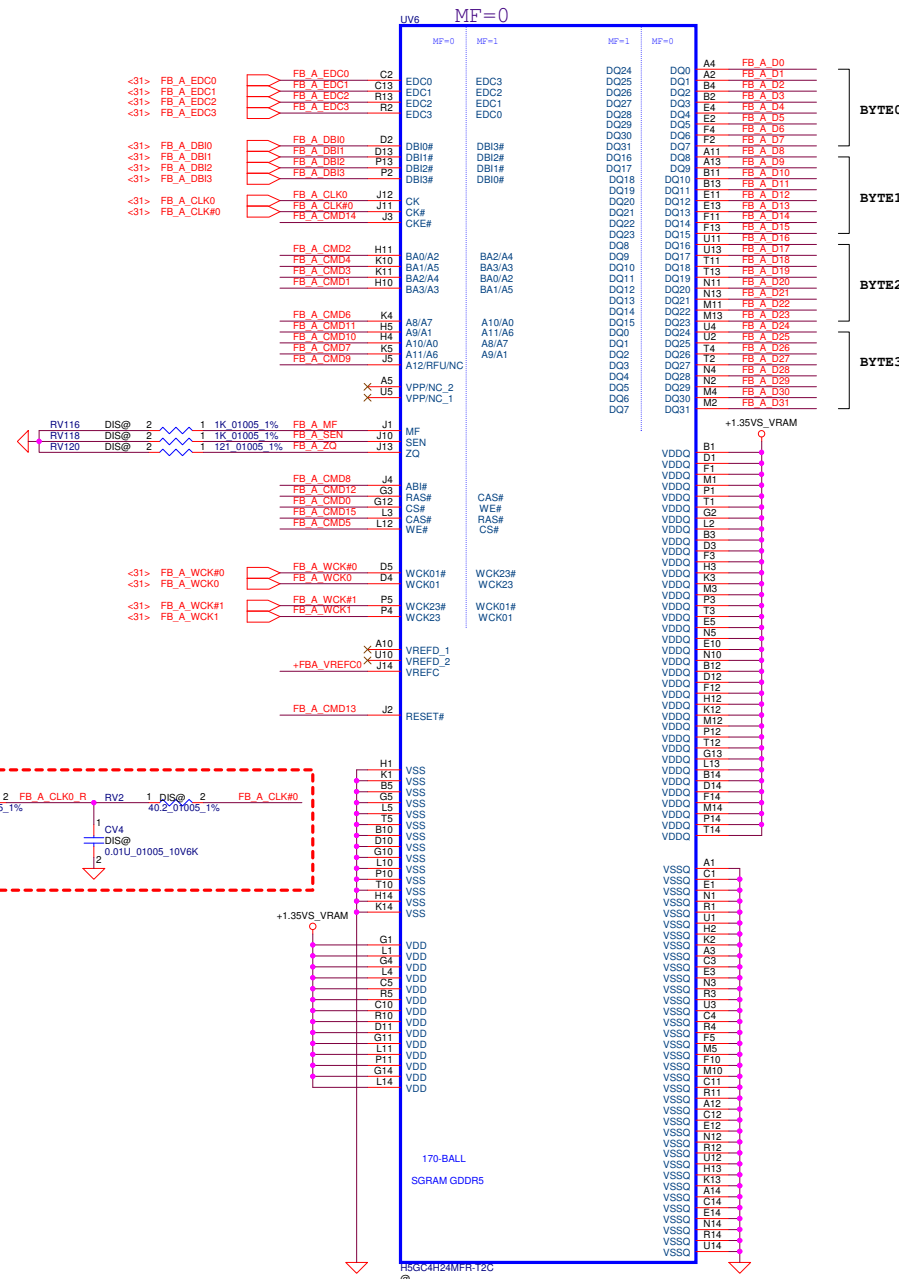
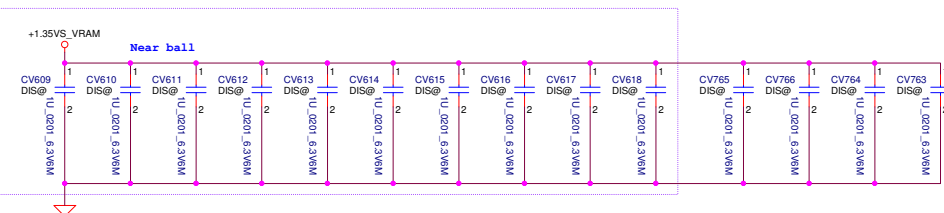
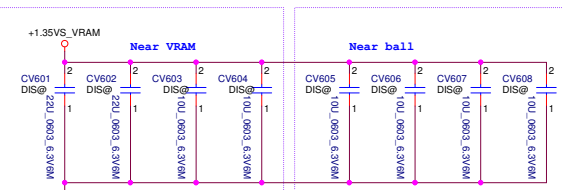
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				Sheet	34 of 100	

Memory Partition A

GB2-64, GB2B-64, GB4B-128	Channel 0 0..31	GB2-64, GB2B-64, GB4B-128	Channel 1 32..63
CMD0	C5*	CMD16	C5*
CMD1	A3_BA3	CMD17	A3_BA3
CMD2	A2_BA0	CMD18	A2_BA0
CMD3	A4_BA2	CMD19	A4_BA2
CMD4	A5_BA1	CMD20	A5_BA1
CMD5	WE*	CMD21	WE*
CMD6	A7_A8	CMD22	A7_A8
CMD7	A6_A11	CMD23	A6_A11
CMD8	ABI*	CMD24	ABI*
CMD9	A12_RFU	CMD25	A12_RFU
CMD10	A0_A10	CMD26	A0_A10
CMD11	A1_A9	CMD27	A1_A9
CMD12	RAS*	CMD28	RAS*
CMD13	RST*	CMD29	RST*
CMD14	CKE*	CMD30	CKE*
CMD15	CA5*	CMD31	CA5*

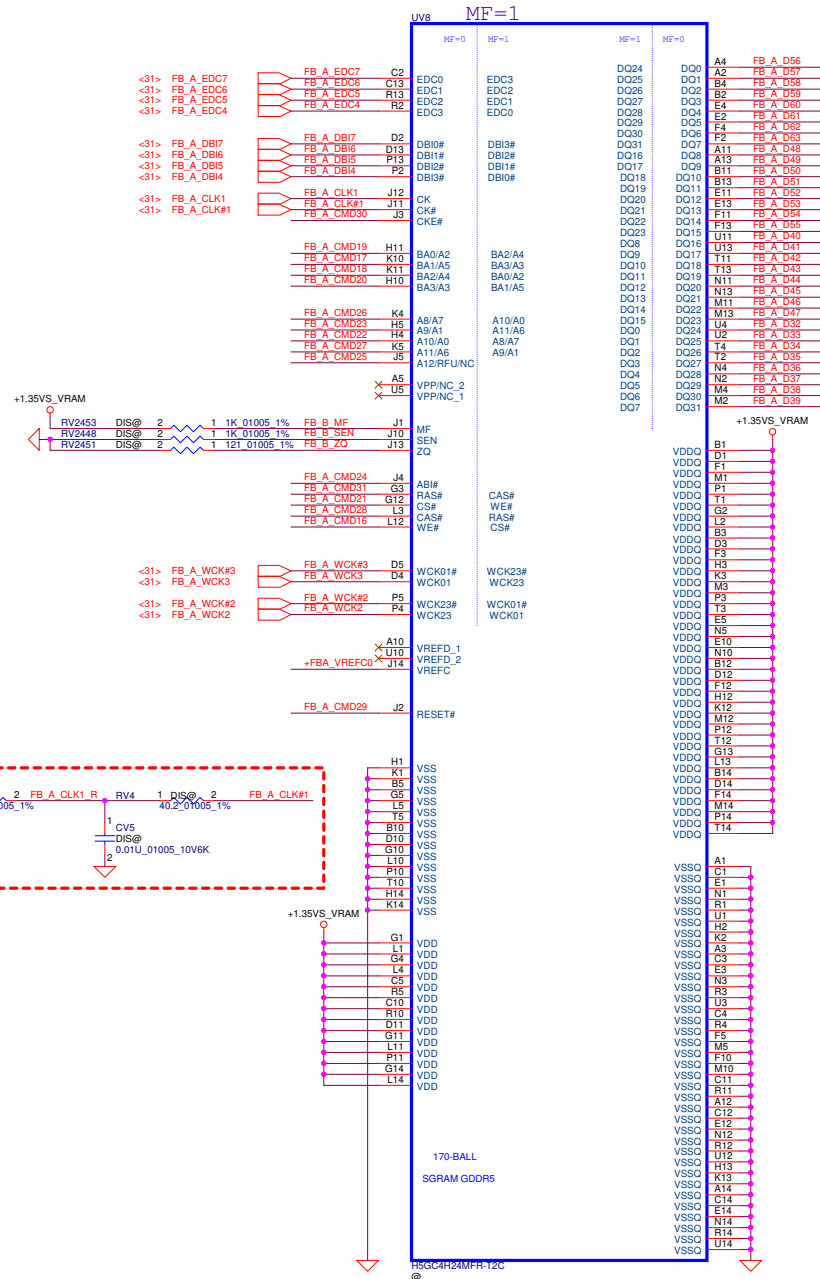
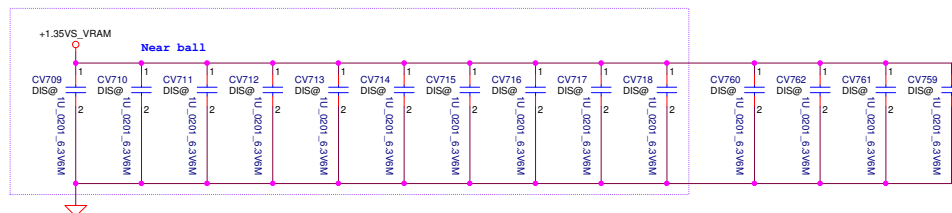
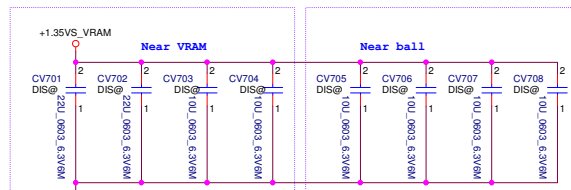
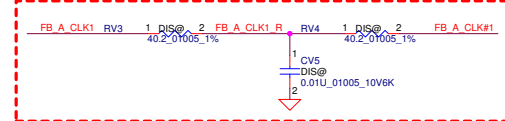
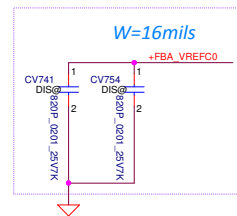
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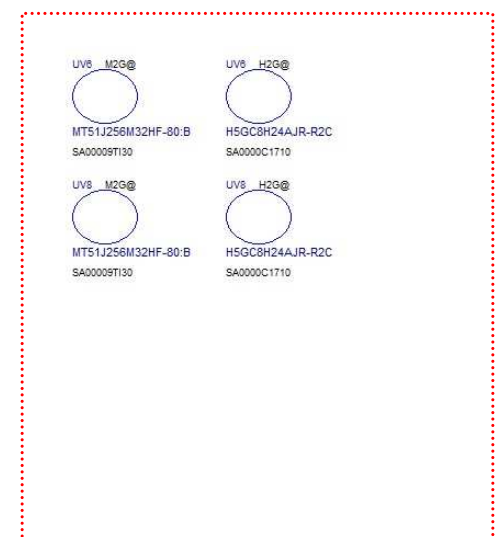
Memory Partition B

GB2-64, GB28-64, GB48-128	Channel 0 0..31	GB2-64, GB28-64, GB48-128	Channel 1 32..63
CMD0	CS*	CMD16	CS*
CMD1	A3_BA3	CMD17	A3_BA3
CMD2	A2_BA0	CMD18	A2_BA0
CMD3	A4_BA2	CMD19	A4_BA2
CMD4	A5_BA1	CMD20	A5_BA1
CMD5	WE*	CMD21	WE*
CMD6	A7_A8	CMD22	A7_A8
CMD7	A6_A11	CMD23	A6_A11
CMD8	ABI*	CMD24	ABI*
CMD9	A12_RFU	CMD25	A12_RFU
CMD10	A0_A10	CMD26	A0_A10
CMD11	A1_A9	CMD27	A1_A9
CMD12	RA5*	CMD28	RA5*
CMD13	RST*	CMD29	RST*
CMD14	CKE*	CMD30	CKE*
CMD15	CAS*	CMD31	CAS*

GB2-64, GB2B-64, GB4B-128	Channel 0 & 1
CMD32	Not used
CMD33 ¹	Not used
CMD34	DEBUG ²
CMD35	DEBUG ²



Check

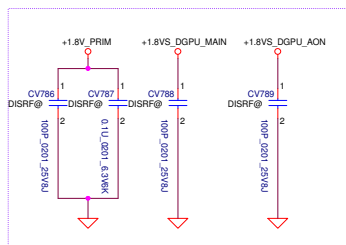


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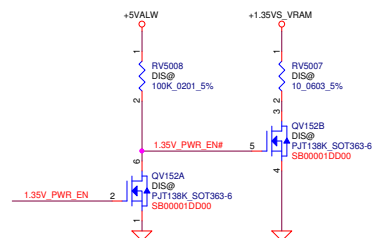
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<11.30> DGPU_PWR_EN
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<31.96> 1.35V_PWR_EN

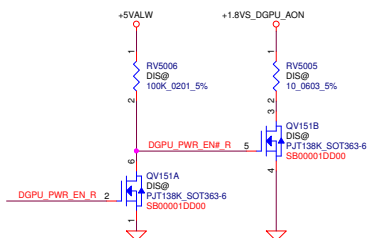
Place near UV2



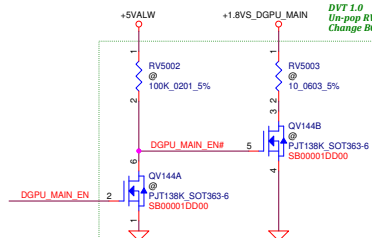
+1.35VS_VRAM Discharge



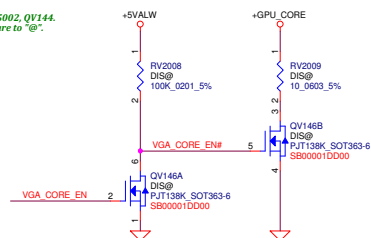
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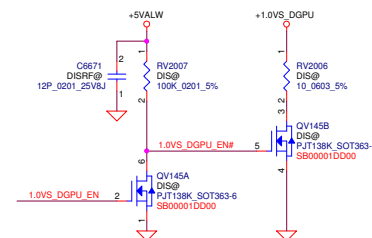
+1.8VS_DGPU_MAIN Discharge



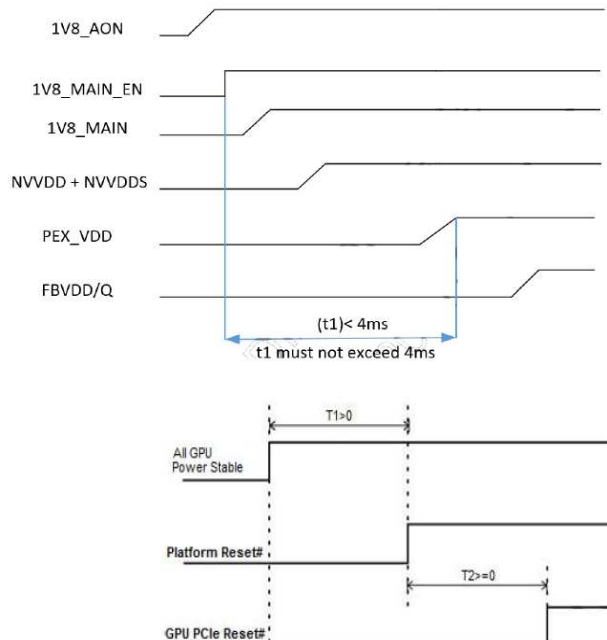
+GPU_CORE Discharge



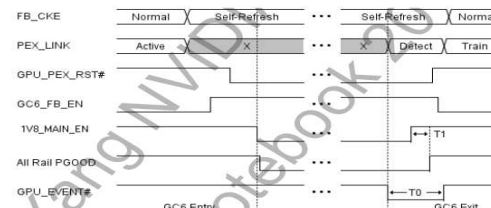
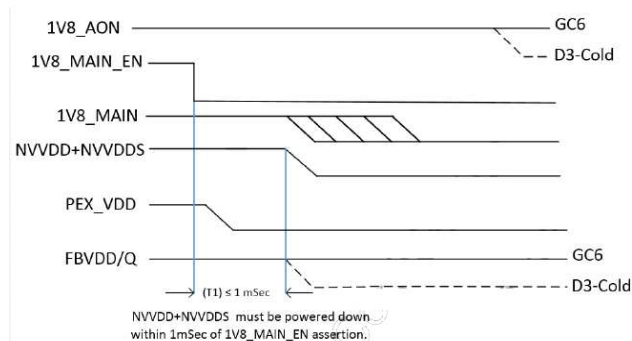
+1.0VS_DGPU Discharge



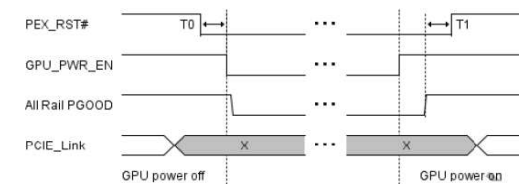
Power-Up Sequence



Power-Down Sequence



Symbol	Description	Min	Max	Units
T0	GPU_EVENT# assertion period	0.001	N/A	ms
T1	1V8_MAIN_EN assertion to all power rails up and stable	0.04	4	ms

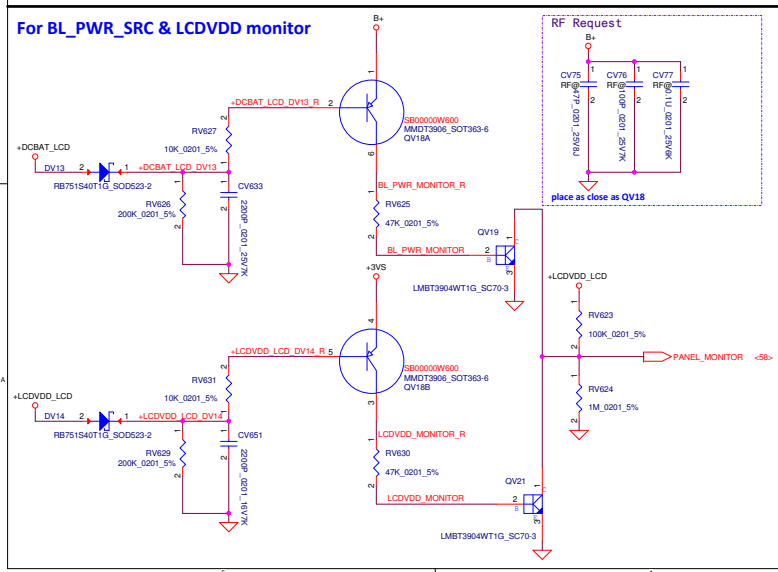
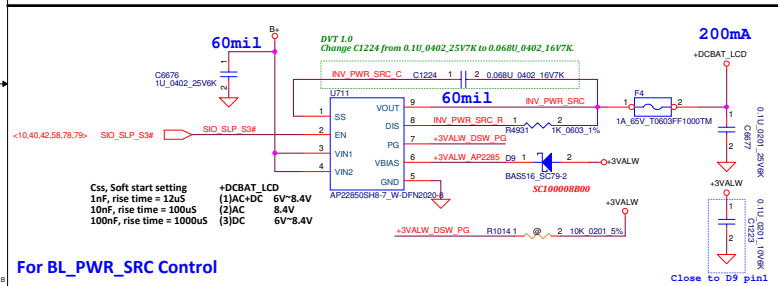
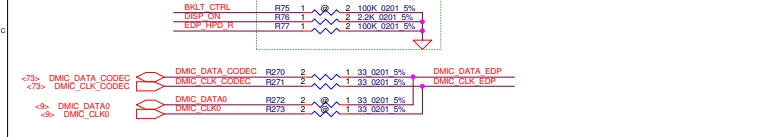
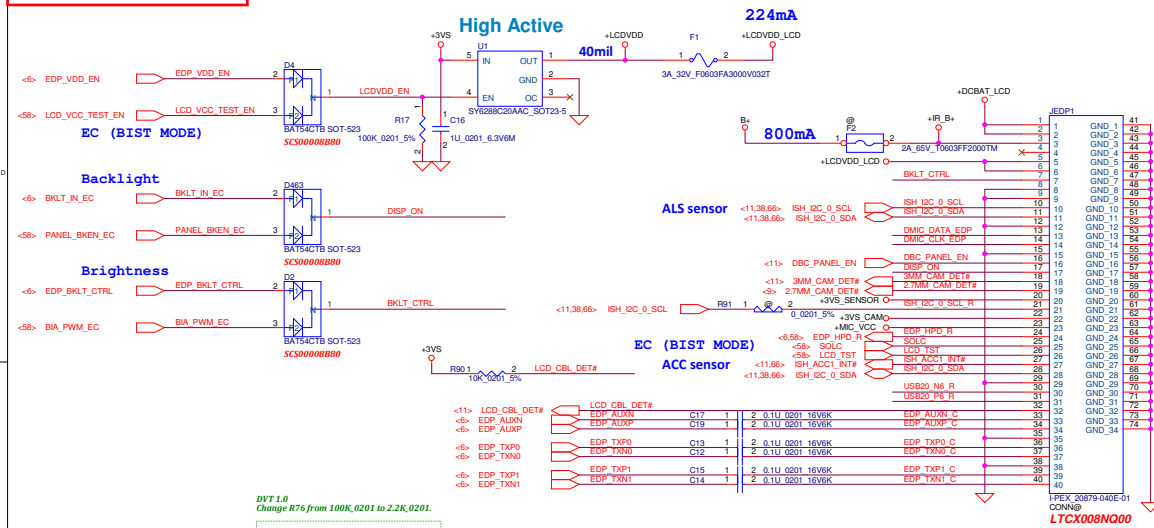


Symbol	Description	Min	Max	Units
T0	PEX_RST# assertion to GPU_PWR_EN=0	>0	5	ms
T1	All GPU power rail up and stable to PEX_RST# de-assertion	0.1	5	ms

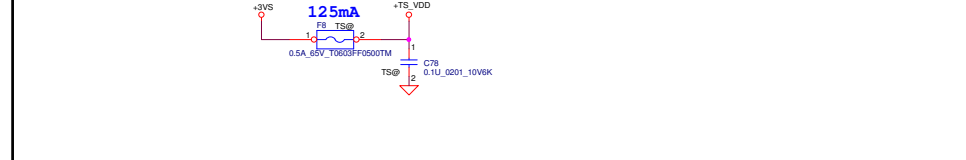
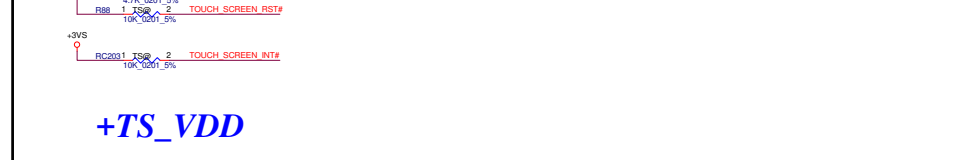
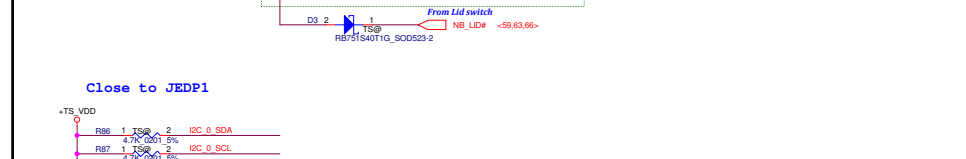
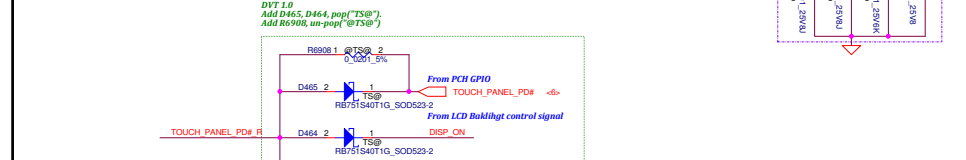
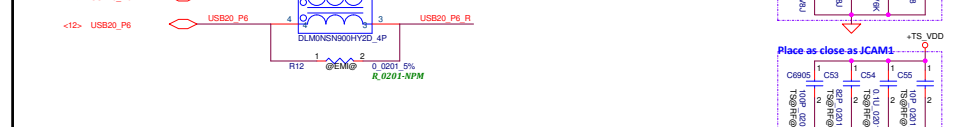
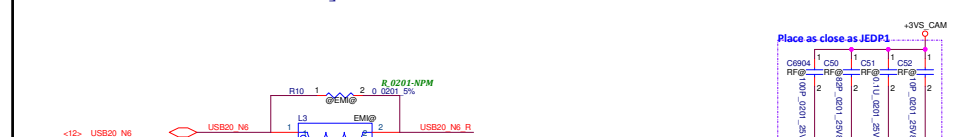
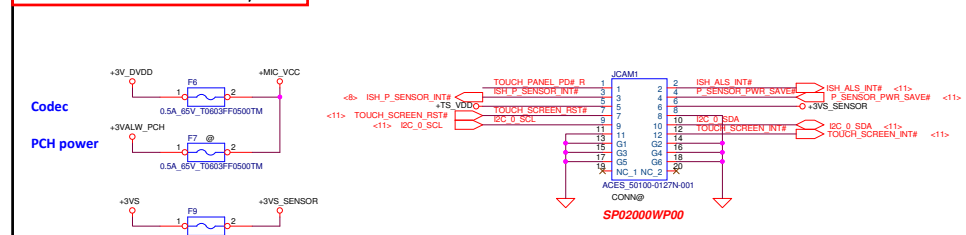
Figure 8.4 Cold Reset Sequence Requirement for Optimus

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Main Func = LCD



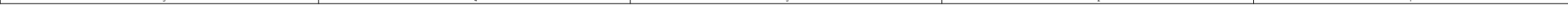
Main Func = CAM, TS



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Date:	Monday, July 15, 2019	Sheet	38	of	100

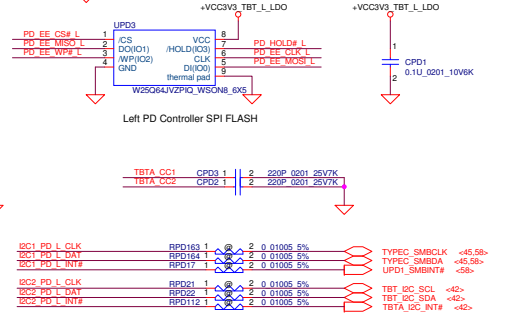
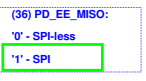
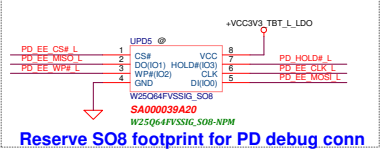
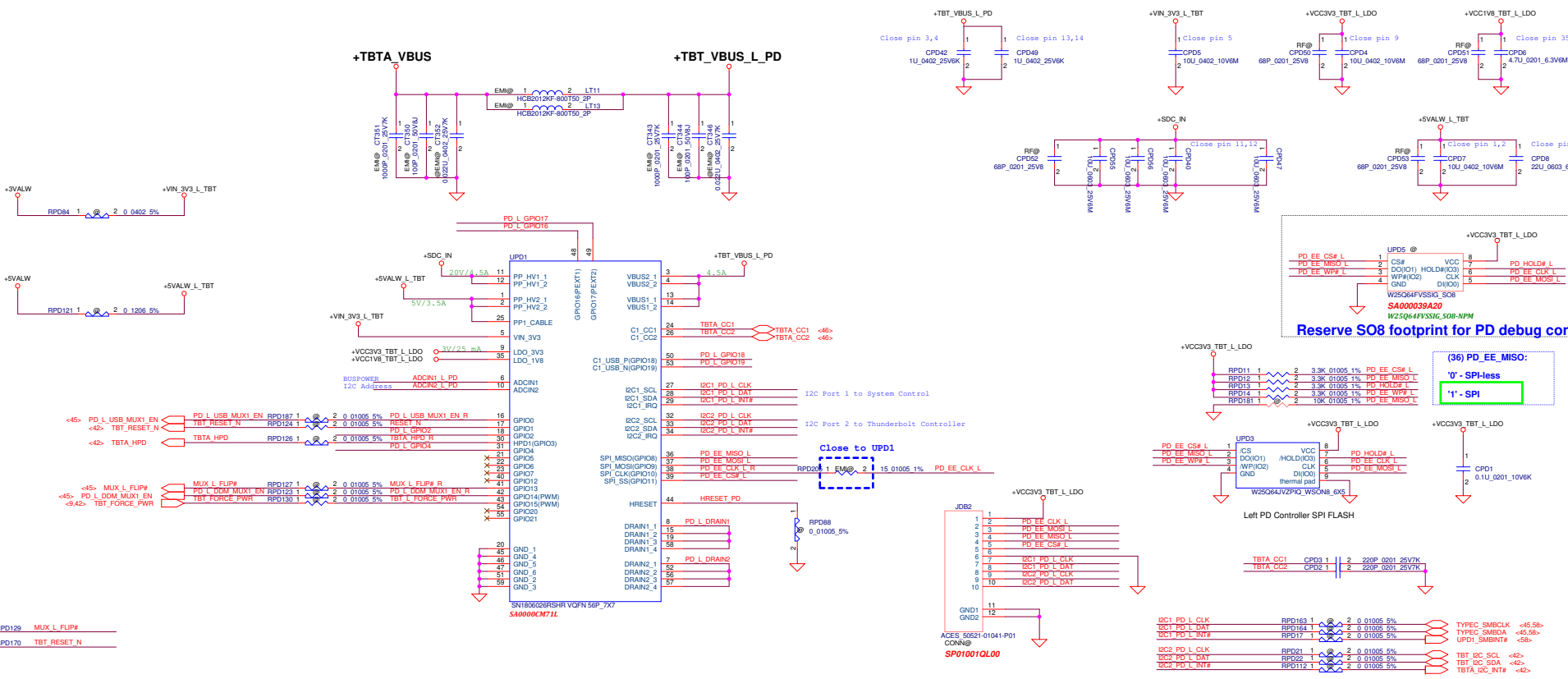
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				Date	Monday, July 15, 2019	Sheet 39 of 100
				LA-H451P		
				1.0		

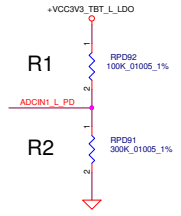


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				Date	Monday, July 15, 2019	1.0
				Sheet	41	of 100

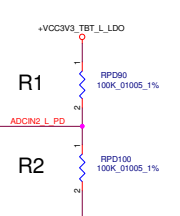


BUSPOWER Config BP_NoWait value 0.7~0.78

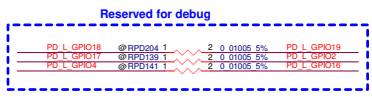


BP min	BP max	Configuration	Description	Recommended for
0.00	0.18	BP_NoWait	BP power switch is enabled and the device does not wake-up and VIN_V3 is support	Ports intended to operate as a USB device only, or applications that do not support charging or operation during a dead battery condition.
0.20	0.38	BP_VinFUSE1_Limit	The internal pull-up from VBUS to BP_VinFUSE1 is limited to the point of no current flow. The device does not attempt to start-up or attempt to load device configuration until VIN_V3 is present.	Ports that support operating as a sink or GND support charging or operation during a dead battery condition, and depend on outside system components for device configuration and operation.
0.40	0.58	BP_VinFUSE2_Limit	The battery power switch from VBUS to BP_VinFUSE2 is enabled for the port. The device does not attempt to start-up or attempt to load device configuration until VIN_V3 is present.	Ports that support operating as a sink or GND support charging or operation during a dead battery condition, and depend on outside system components for device configuration and operation.
0.60	1.00	BP_NoWait	The device continues to start-up and attempts to load configuration while waiting power from VBUS. Once configuration is loaded the appropriate power source is chosen based on the loaded configuration.	Ports that support operating as a sink or GND support charging or operation during a dead battery condition, and do not depend on outside system components for device configuration and operation.

I2C Address Divider:010b



BP min	BP max	PC Address Selection	PC Address
0.00	0.18	PC Address Selection	PC Address
0.20	0.38	PC Address Selection	PC Address
0.40	0.58	PC Address Selection	PC Address
0.60	1.00	PC Address Selection	PC Address



The schematic diagram illustrates the electrical connections between the USB20 module and the TSSDS10224RUKR_WOFN20_3x3. Key components and connections include:

- Power Supply:**
 - +3VALW:** Connected to pin 2 of the USB20 module and pin 13 (VCC) of the TSSDS10224RUKR_WOFN20_3x3.
 - GND:** Connected to pin 1 of the USB20 module and pin 5 (GND) of the TSSDS10224RUKR_WOFN20_3x3.
- Signal Connections:**
 - SW_USB20_1_P3 and SW_USB20_1_N3:** Connected to pins 1 and 2 of the USB20 module.
 - MUX_L_FLIP# and PD_L_DDM_MUX1_EN:** Connected to pins 3 and 4 of the USB20 module.
 - MUX_L_FLIP# and PD_L_USB_MUX1_EN:** Connected to pins 5 and 6 of the USB20 module.
- Data Connections:**
 - A1_OUTp and A1_OUTn:** Connected to pins 17 and 18 of the USB20 module.
 - A0_OUTp and A0_OUTn:** Connected to pins 19 and 20 of the USB20 module.
 - B1_OUTp and B1_OUTn:** Connected to pins 21 and 22 of the USB20 module.
 - B0_OUTp and B0_OUTn:** Connected to pins 23 and 24 of the USB20 module.
 - SBO_UM4:** Connected to pin 25 of the USB20 module.

Channel	INA	INE
Signal Name	TOP	BOT

					I2C	USB		
ENA	ENB	SAI	SBI	SAO	OUTA0	OUTB0	Mux Functional Mode	PD Controller W/DDM
0	1	–	0	–	Hi-Z	TOP	–	USB only on TOP
0	1	–	1	–	Hi-Z	BOT	–	USB only on BOT
1	1	0	0	0	BOT	TOP	Crosspoint Switch	USB on TOP W/DDM
1	1	1	1	0	TOP	BOT	Crosspoint Switch	USB on BOT W/DDM

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P42-USB MUX

Document Number

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Type-C connector

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				LA-H451P	
				Date: Monday, July 15, 2019	Sheet 46 of 100

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				Date	Monday, July 15, 2019	1.0
				Sheet	47	of 100

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				Date	Monday, July 15, 2019	Sheet 48 of 100
				LA-H451P		
				1.0		

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				LA-H451P	1.0
				Date: Monday, July 15, 2019	Sheet 49 of 100

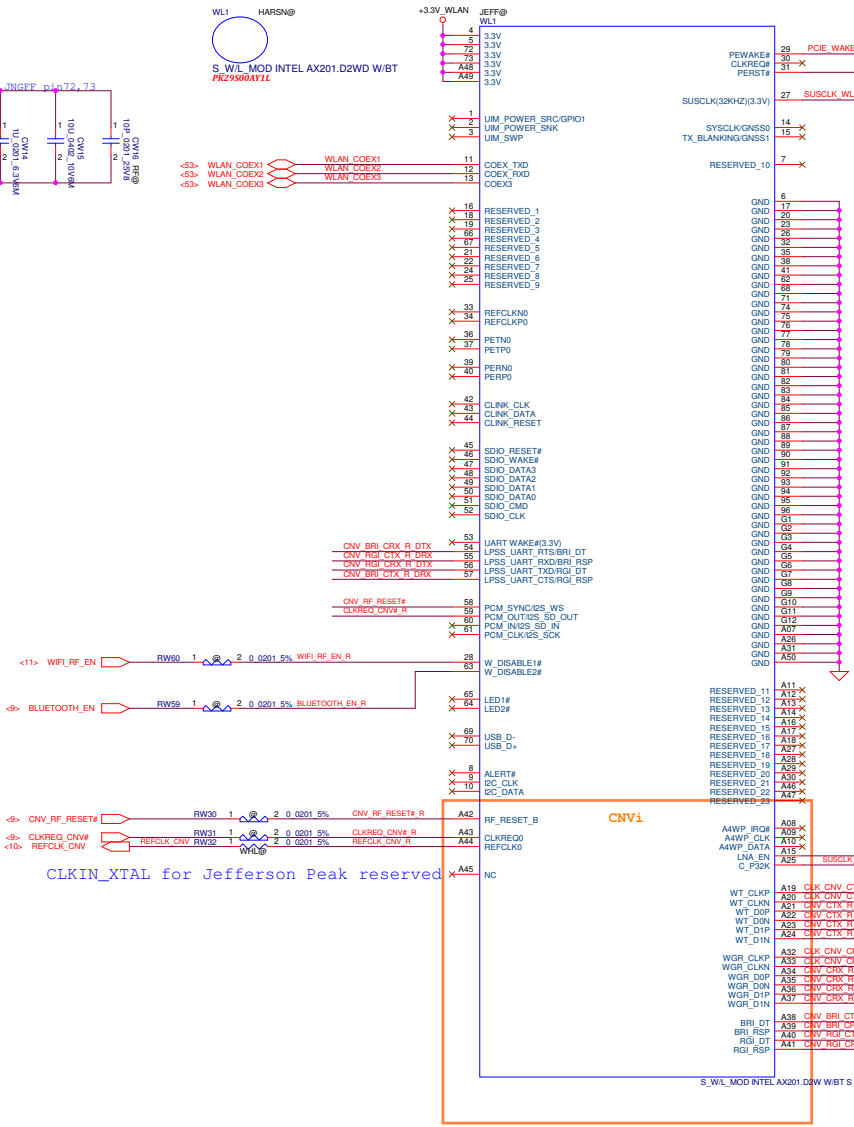
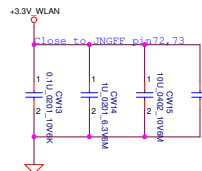
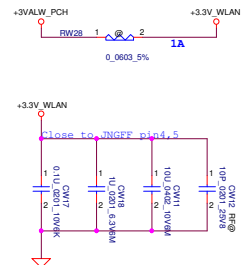
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				Date	Monday, July 15, 2019	Sheet 50 of 100
				LA-H451P		
				1.0		

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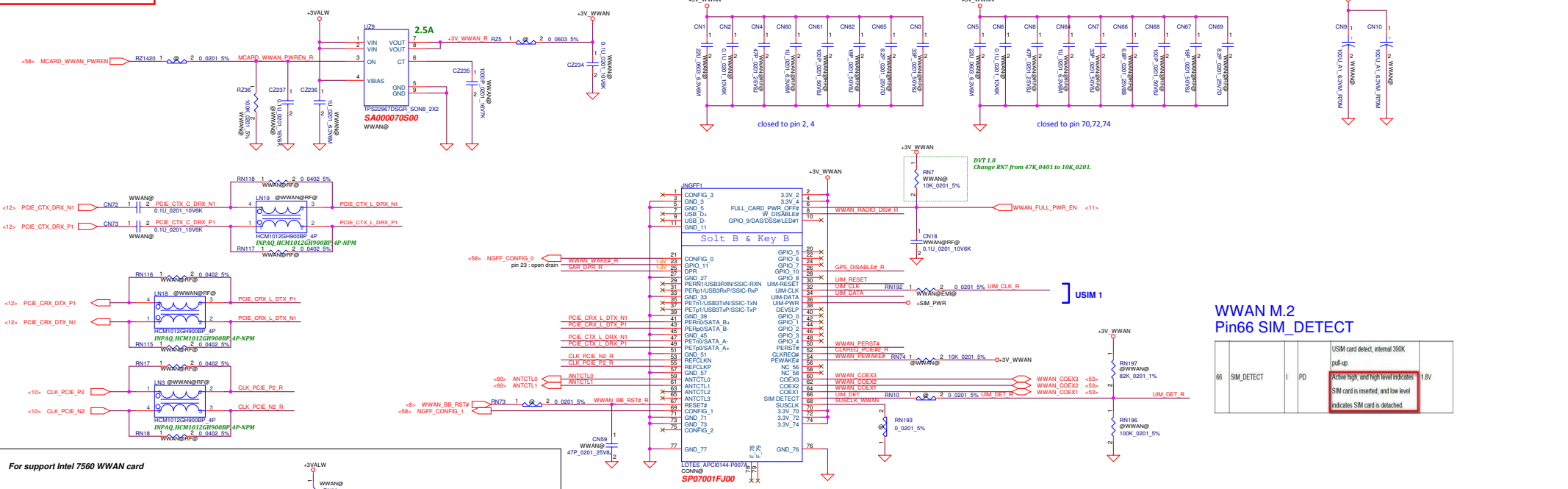
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				Custom	LA-H451P	1.0
Date: Monday, July 15, 2019				Sheet	51	of 100

Main Func = WLAN



RW27,RW25 close to CPU

Main Func = WWAN



For support Intel 7560 WWAN card

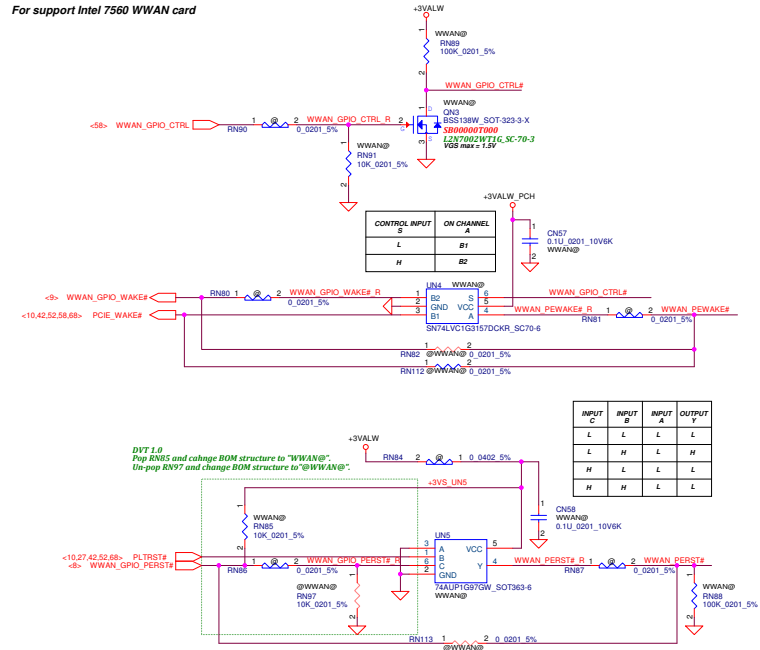


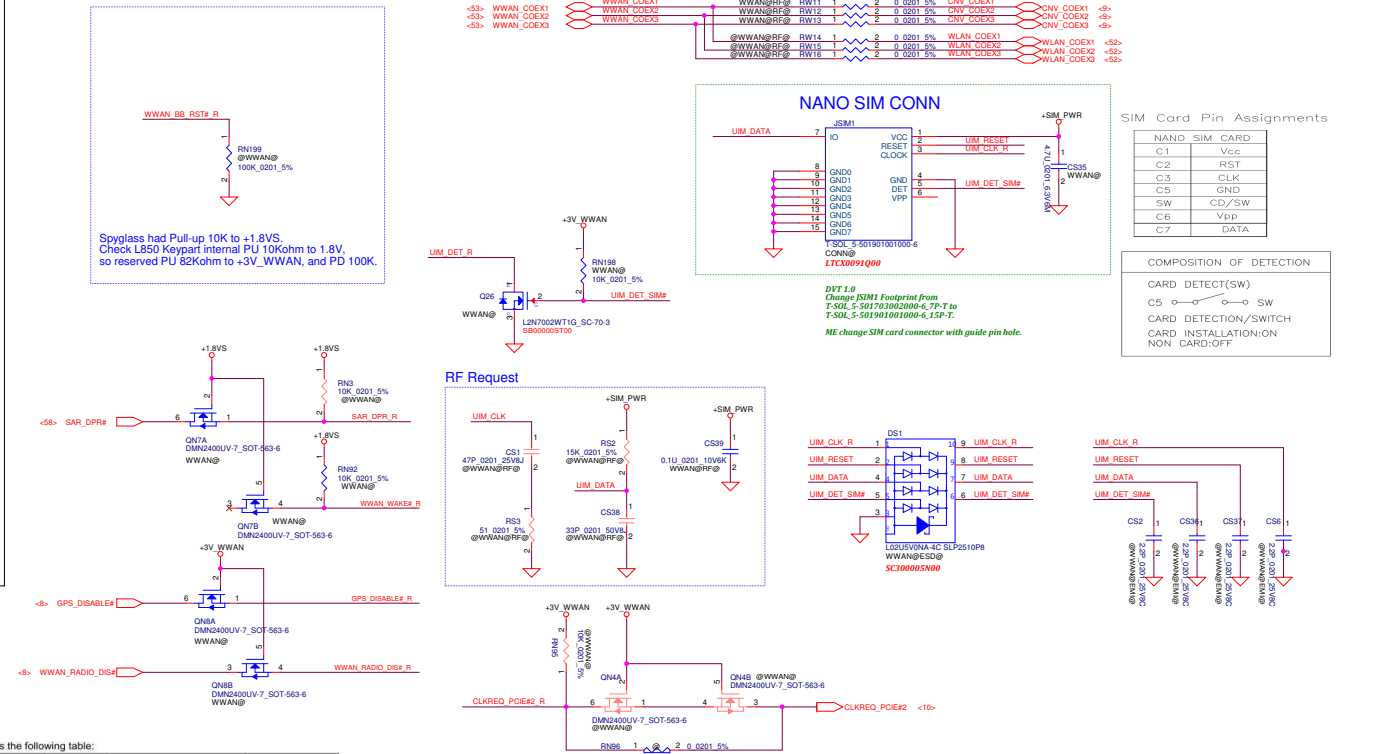
Table 29. Socket 2 Add-in Card Configuration

State #	Add-in Card Configuration Decodes				Add-in Card Type and Main Host Interface (see Note 1)	Port Configuration (see Note 2)
	CONFIG_0 (Pin 21)	CONFIG_1 (Pin 69)	CONFIG_2 (Pin 75)	CONFIG_3 (Pin 1)		
0	GND	GND	GND	GND	SSD – SATA	N/A
1	GND	NC	GND	GND	SSD – PCIe	N/A
2	GND	GND	NC	GND	WWAN – PCIe	0
3	GND	NC	NC	GND	WWAN – PCIe	1
4	GND	GND	GND	NC	WWAN – USB3.1 Gen1	0
5	GND	NC	GND	NC	WWAN – USB3.1 Gen1	1
6	GND	GND	NC	NC	WWAN – USB3.1 Gen1	2
7	GND	NC	NC	NC	WWAN – USB3.1 Gen1	3

FIBOCOM_L850

The M.2 module configuration as the following table:

Config_0 (pin21)	Config_1 (pin69)	Config_2 (pin75)	Config_3 (pin1)	Module Type and Main Host Interface	Port Configuration
GND	GND	GND	NC	WWAN-USB3.1, PCIe Gen1	0



SIM Card Pin Assignments

NANO	SIM	CARD
C1		Vcc
C2		RST
C3		CLK
C5		GND
SW		CD/SW
C6		Vdp
C7		DATA

COMPOSITION OF DETECTION

CARD DETECT(SW)

CARD DETECTION/SWITCH

CARD INSTALLATION:ON
NON CARD:OFF

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				Date	Monday, July 15, 2019	Sheet 54 of 100
				LA-H451P		
				1.0		

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				Date:	Monday, July 15, 2019	Sheet 55 of 100

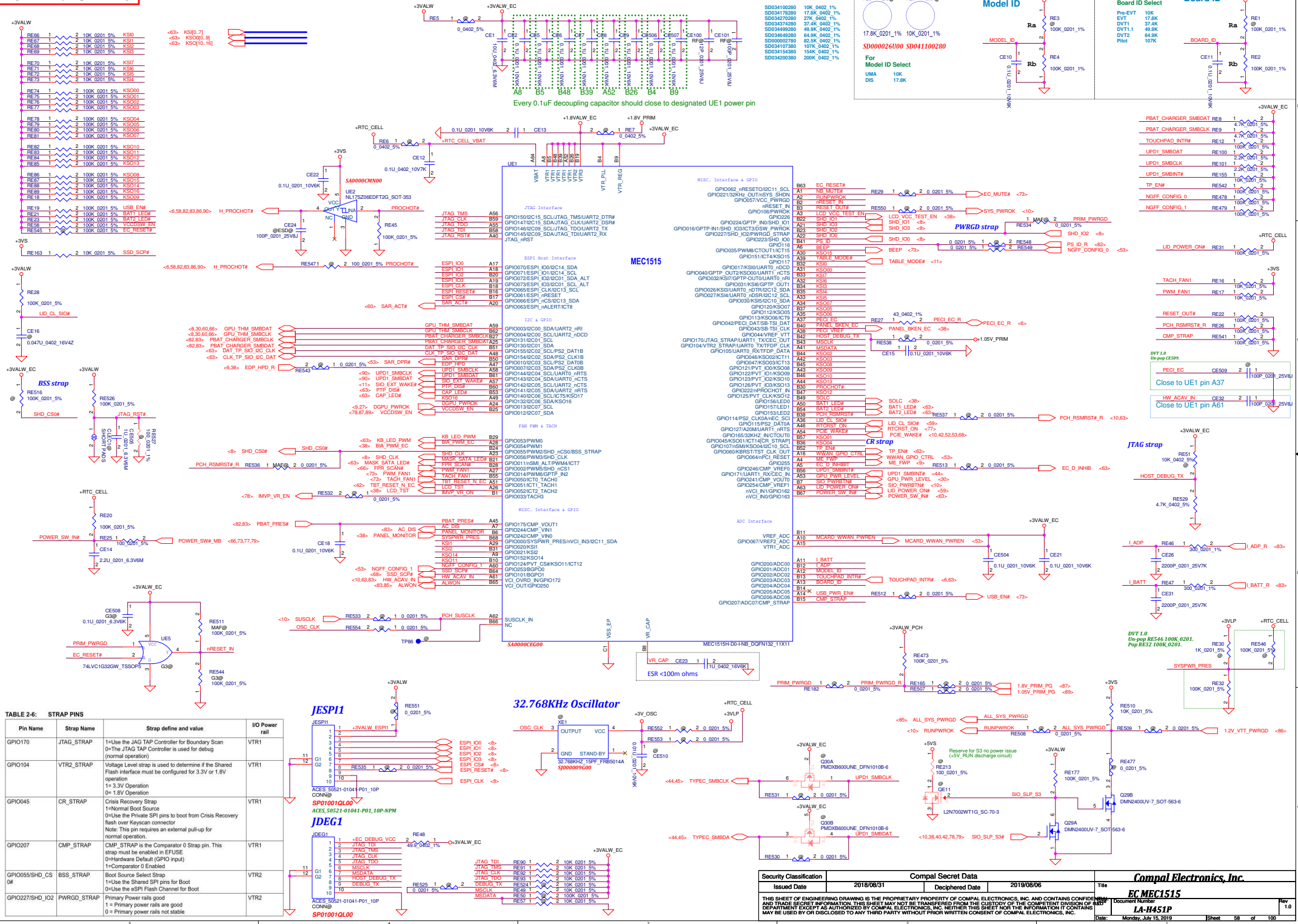
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				Date	Monday, July 15, 2019	Sheet 56 of 100
				LA-H451P		
				1.0		

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				Date	Monday, July 15, 2019	1.0
				Sheet	57 of 100	

Main Func = EC

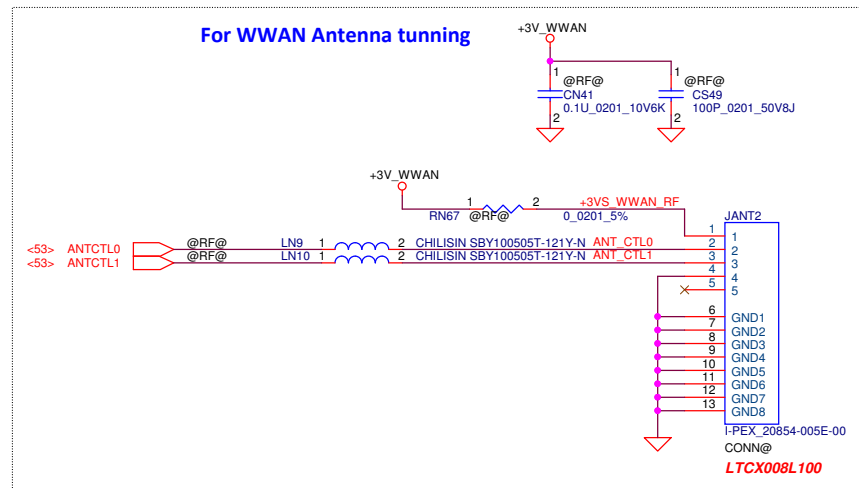
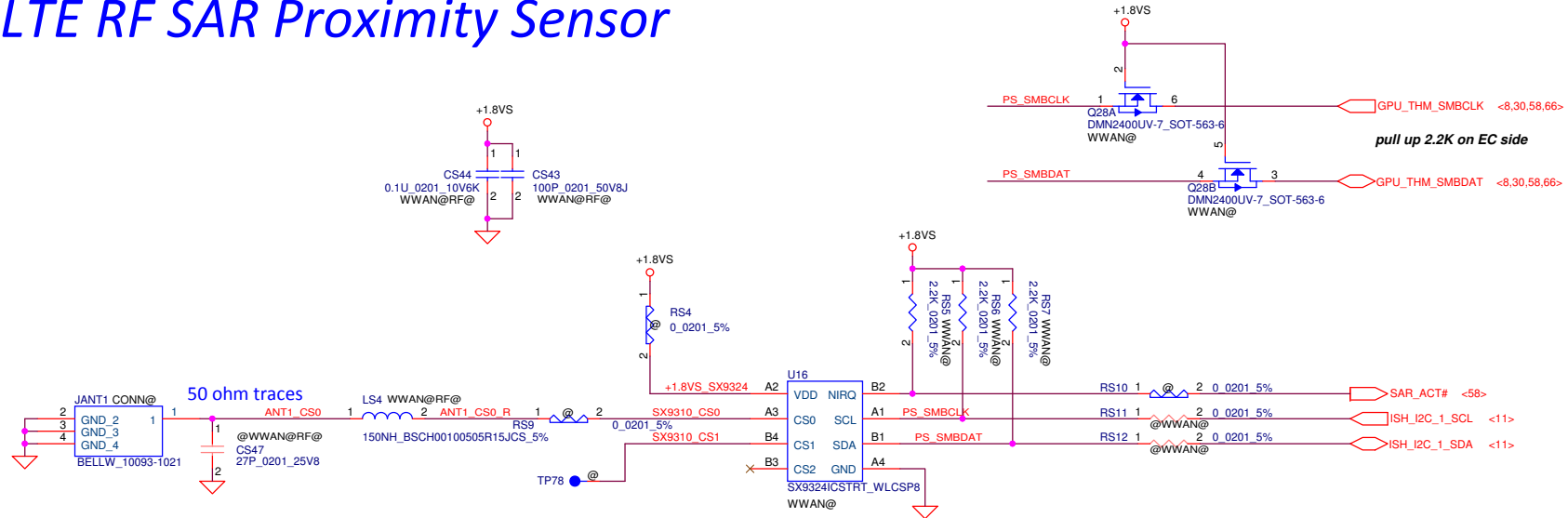


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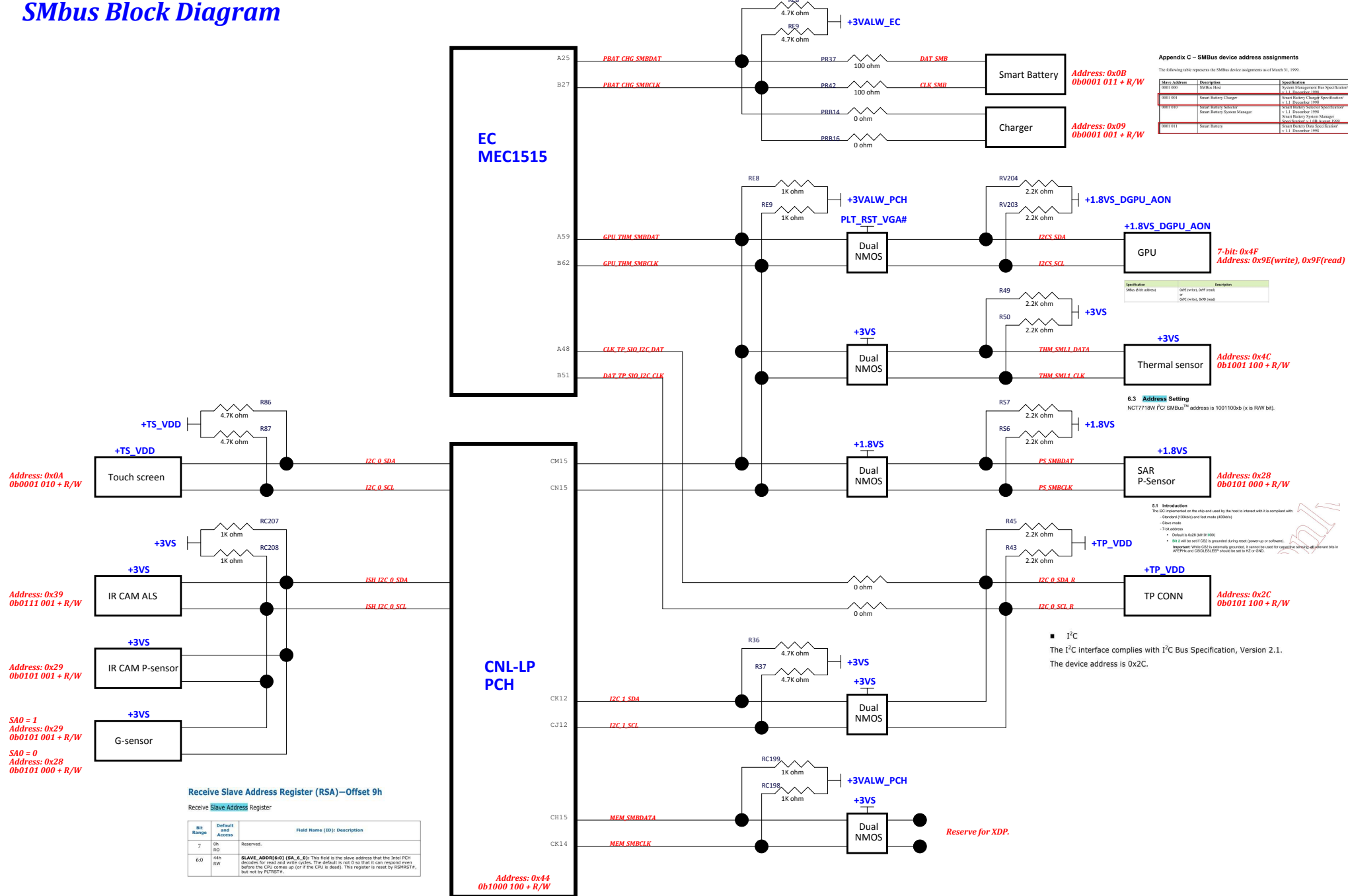
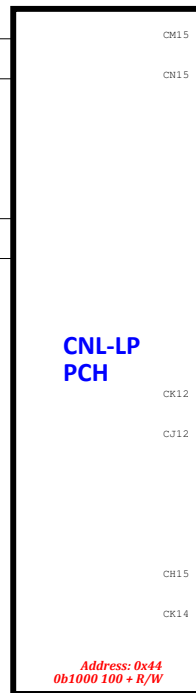
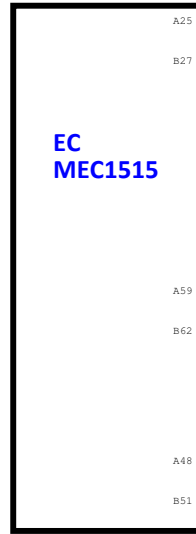
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LTE RF SAR Proximity Sensor



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				Date	Monday, July 15, 2019
				Sheet	60 of 100
				Rev	1.0

SMbus Block Diagram



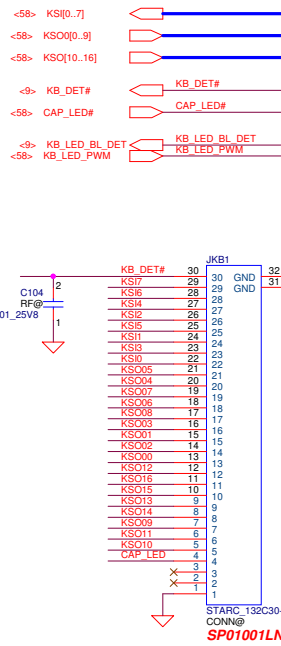
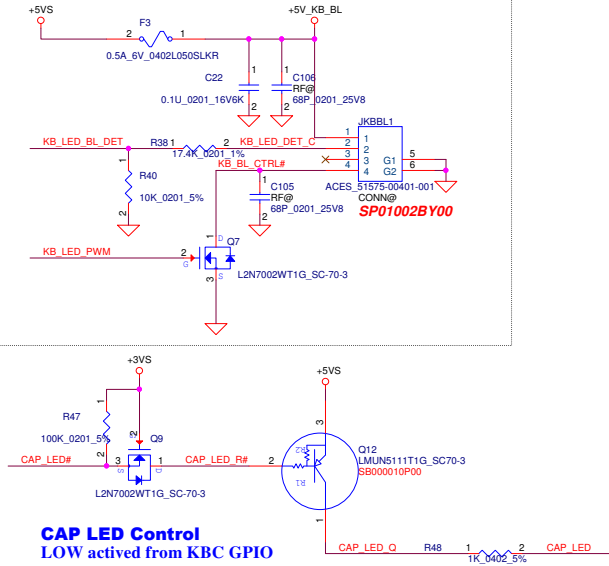
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				Date	Monday, July 15, 2019	Sheet 62 of 100
				LA-H451P		
				1.0		

Main Func = KB/KBBL

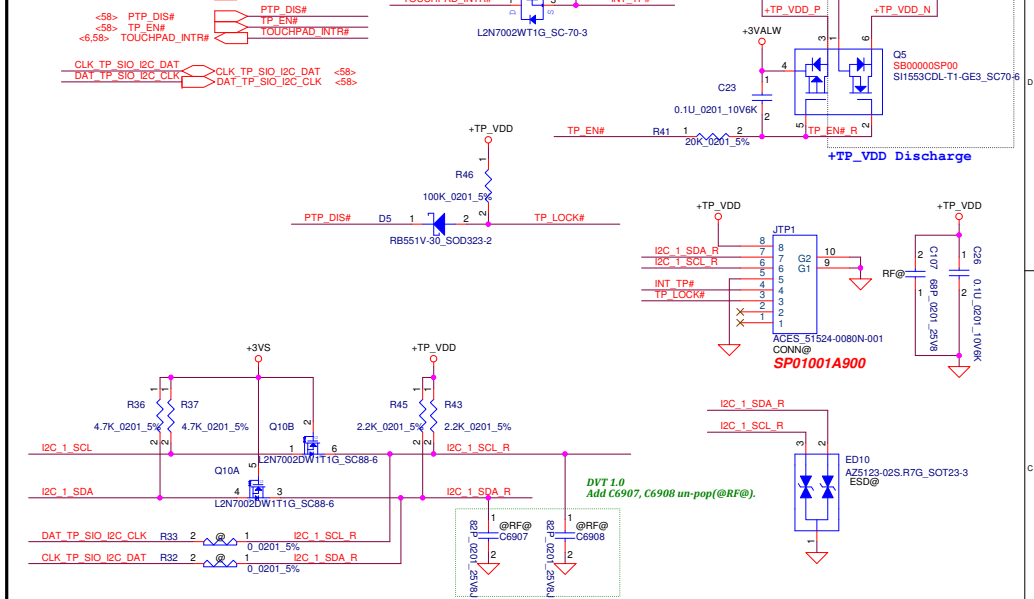
Keyboard Backlight

KB Backlight Power Consumption: 400mA max.

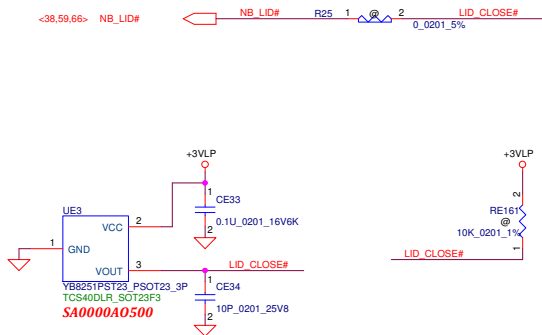


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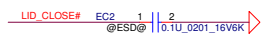
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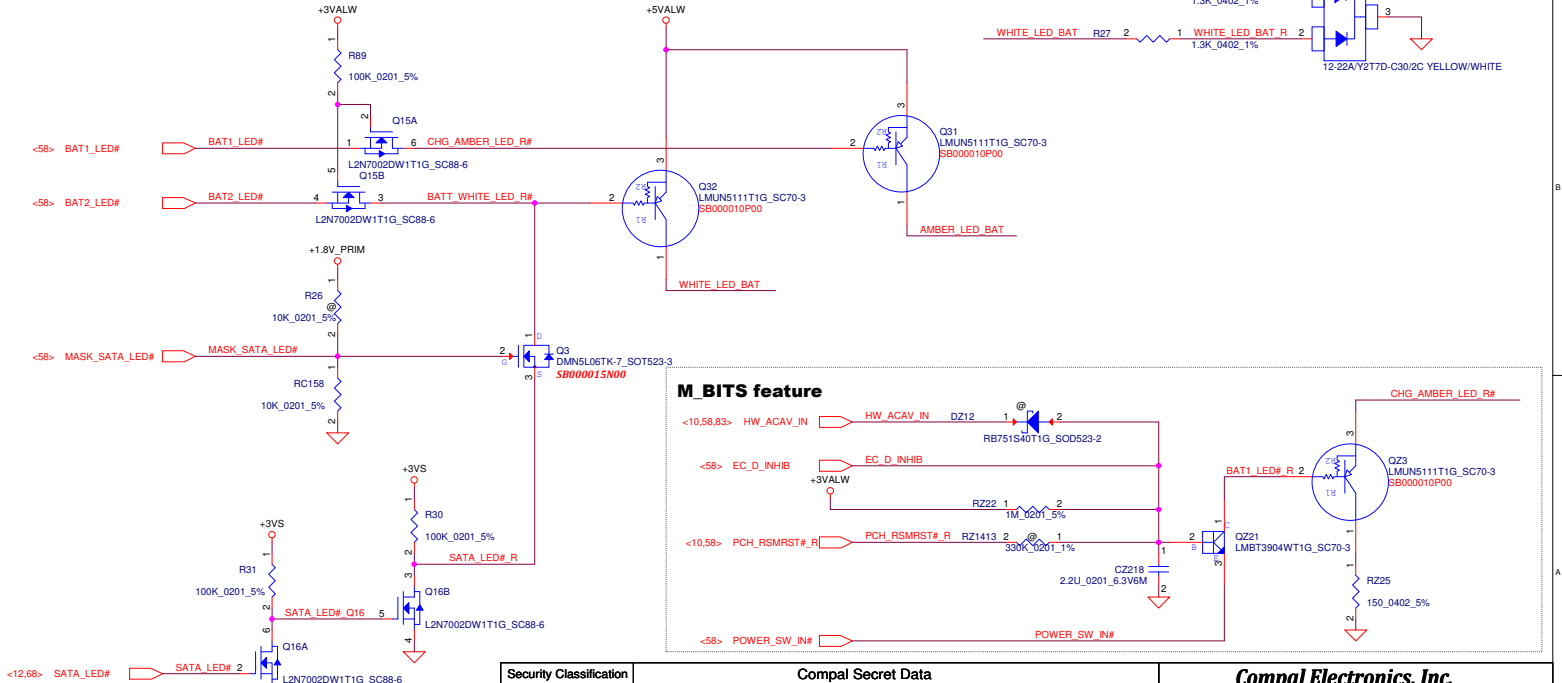
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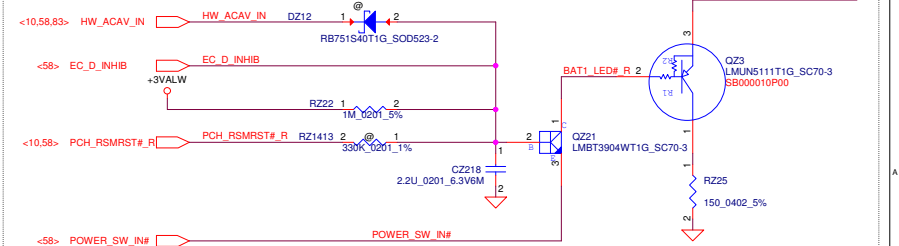
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Main Func = Battery LED



M_BITS feature



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Date:	Monday, July 15, 2019	Sheet	63	of 100

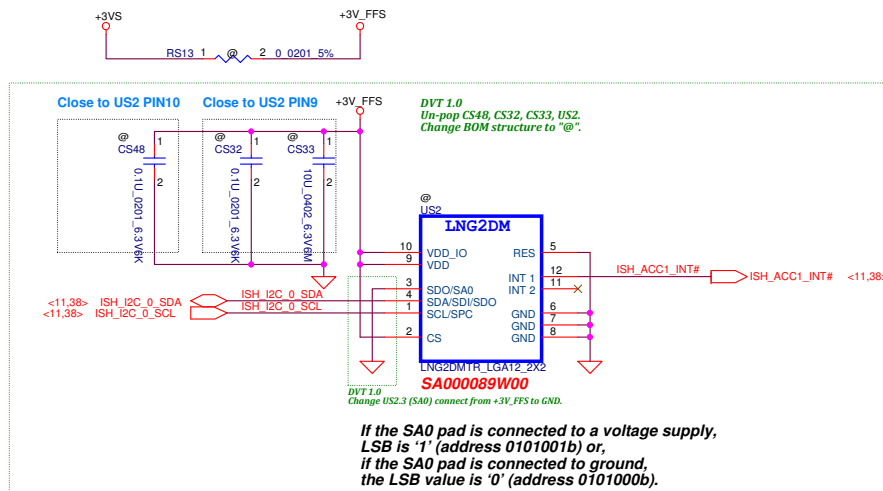
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				Date	Monday, July 15, 2019	1.0
				Sheet	64 of 100	

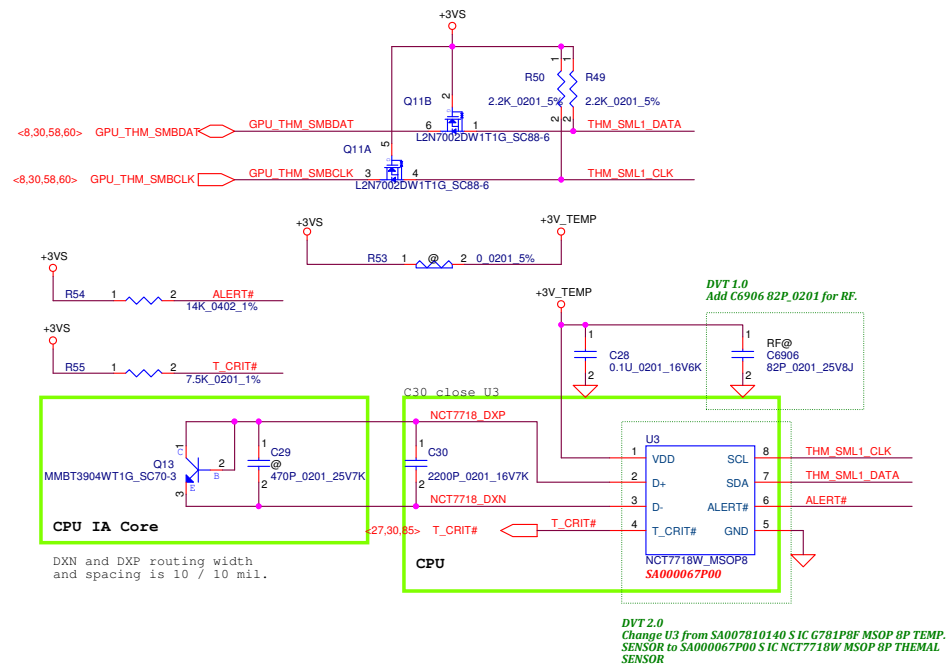
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				Date	Monday, July 15, 2019	Sheet 65 of 100
				LA-H451P		
				1.0		

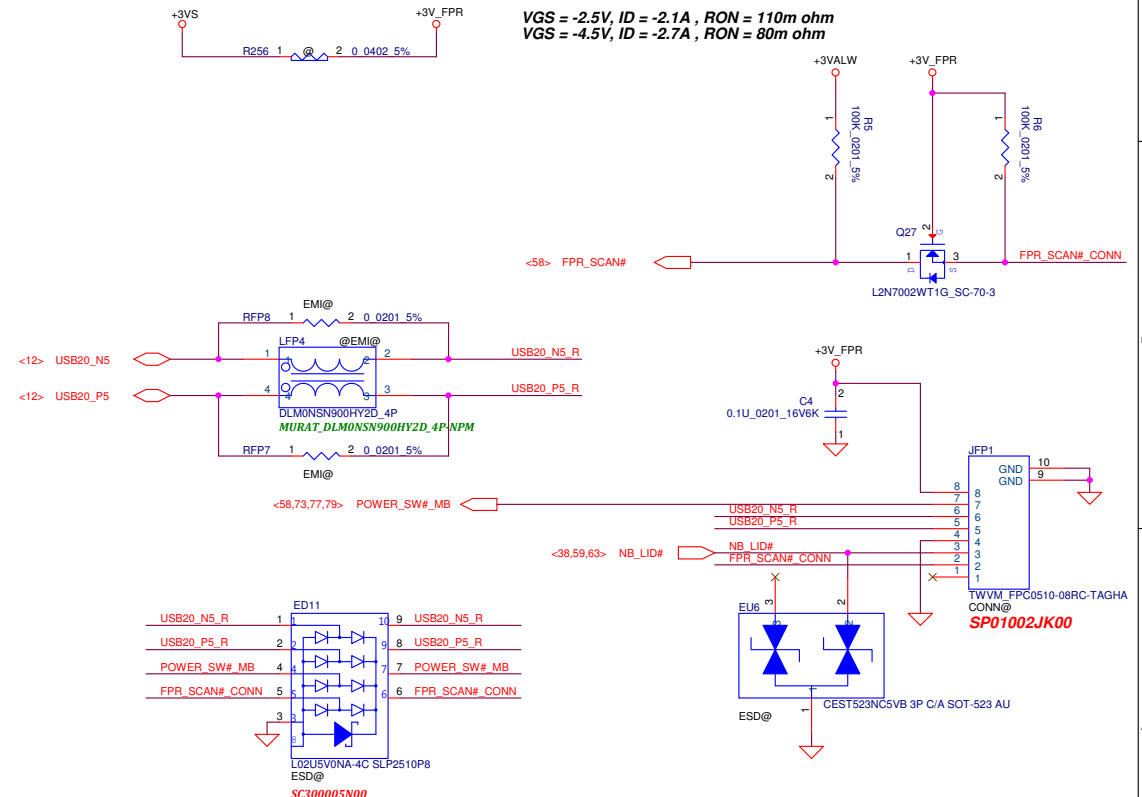
Main Func = G-Sensor



Main Func = Thermal



Main Func = Finger Printer



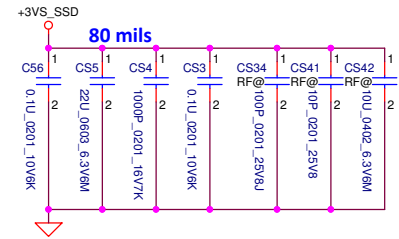
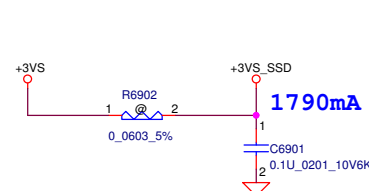
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						Document Number		LA-H451P		Rev	
						Date: Monday, July 15, 2019		Sheet 66 of 100		1.0	

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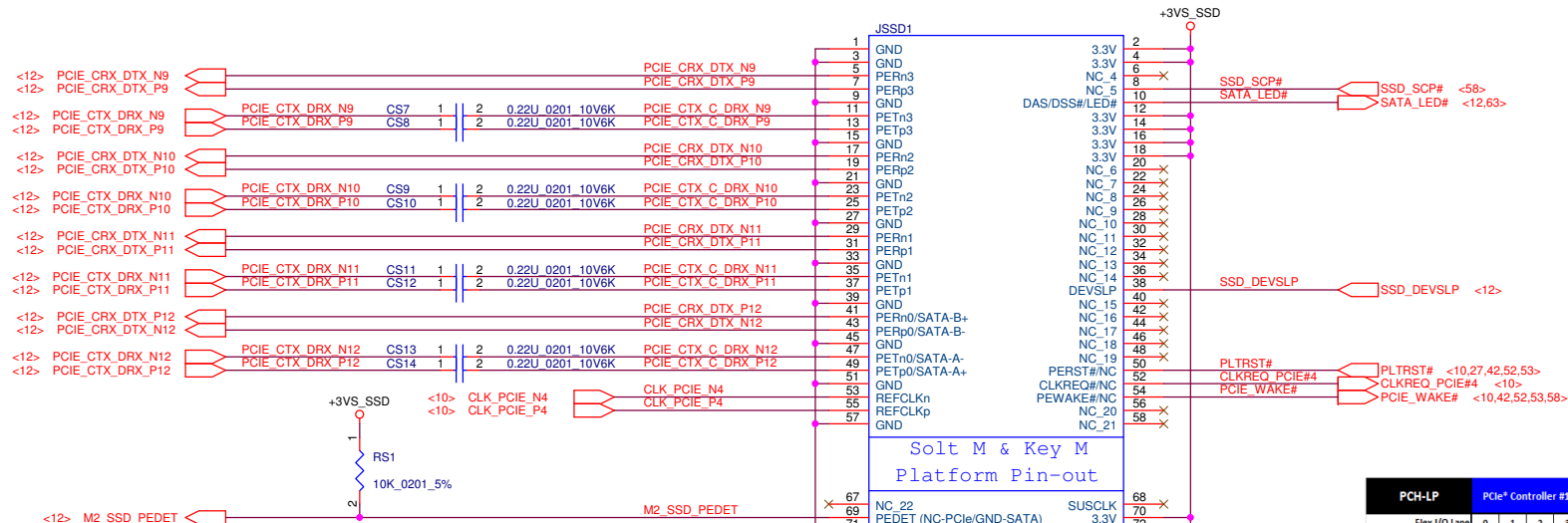
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				Custom	LA-H451P	1.0
				Date:	Monday, July 15, 2019	Sheet 67 of 100

Main Func = SSD

Key M CONN



NGFF Key M



PEDET	Module Type
0	SATA
1	PCIE

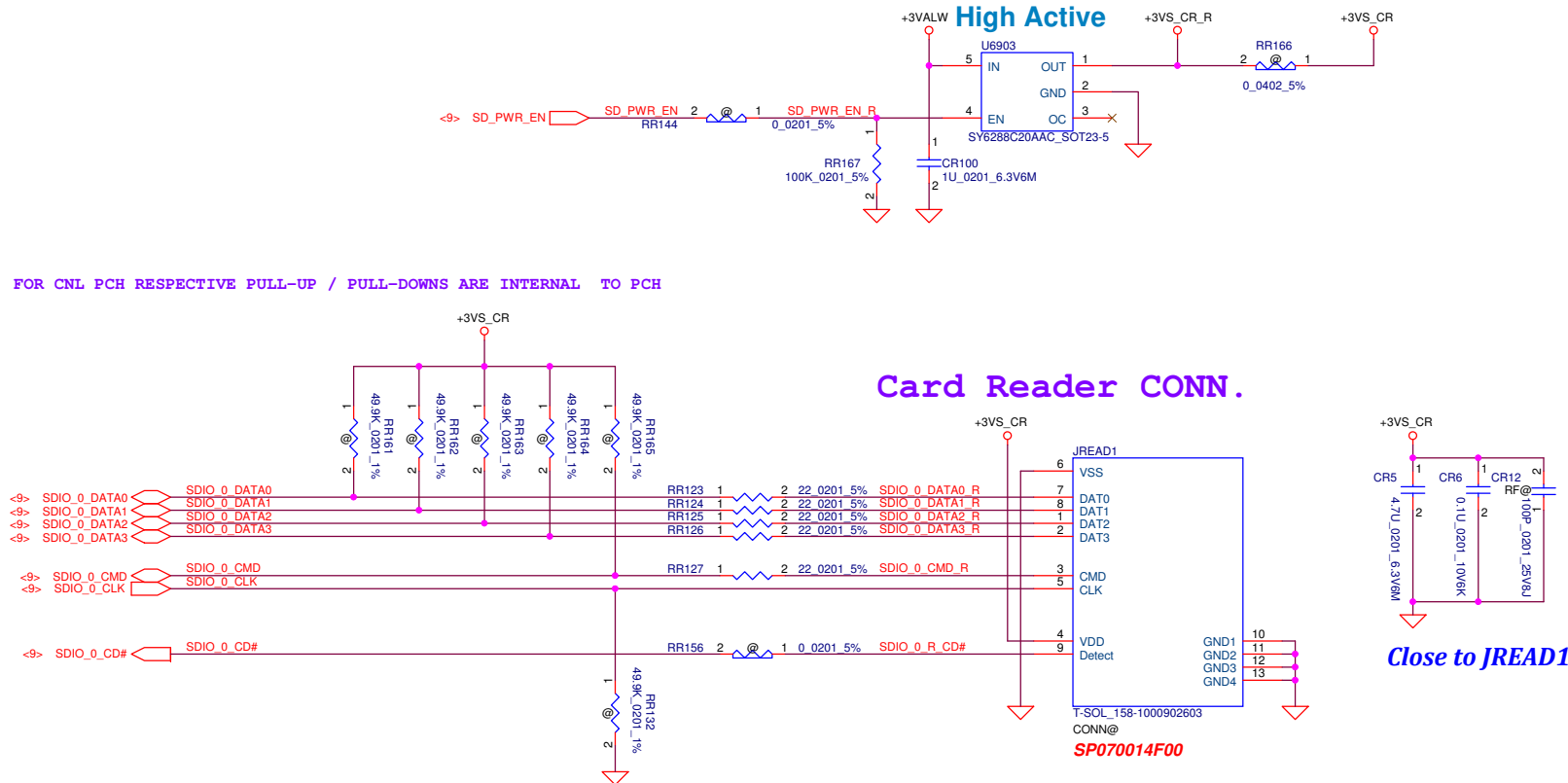
PCH-LP	PCIe* Controller #1				PCIe* Controller #2				PCIe* Controller #3				PCIe* Controller #4			
	Cycle Router #2				Cycle Router #3				Cycle Router #4				Cycle Router #5			
Flex I/O Lane	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
PCIe* Lane	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Base-U	1x4 LR															
	2x2															
	1x2+2x1															
	2x1+1x2															
Premium-U	1x4 LR															
	2x2															
	1x2+2x1															
	2x1+1x2															
Premium-Y	1x4 LR															
	2x2															
	1x2+2x1															
	2x1+1x2															

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		Sheet		68		of		100	
		Rev		1.0					

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				Document Number	Rev
				LA-H451P	1.0
Date: Monday, July 15, 2019				Sheet	69 of 100

Main Func = Card Reader



Opening/Close of Switch

Card Detect Switch	
Card Uninsertion	Open
Card Half Insertion	Open
Card Insertion	Close
N/O	Open Close

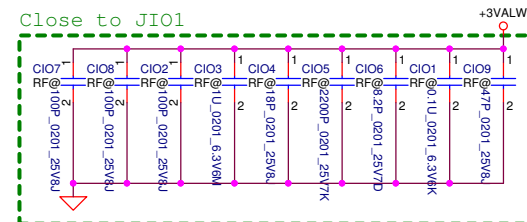
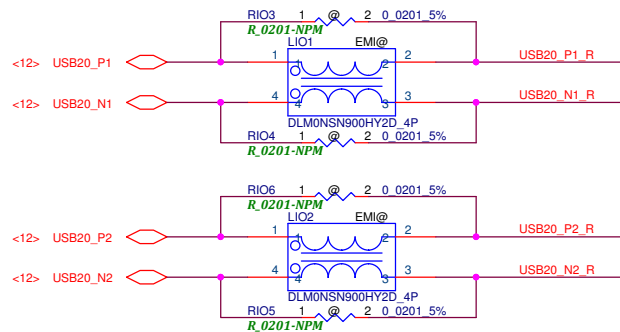
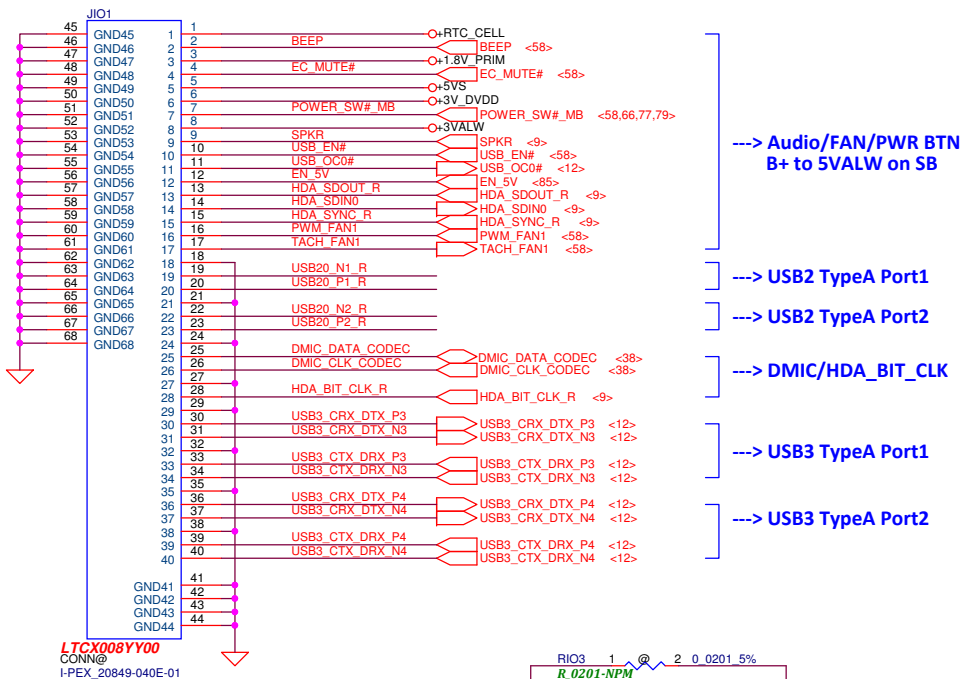
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Issued Date	2018/08/31	Deciphered Date	2019/08/06	Title	
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Date: Monday, July 15, 2019				Sheet 70	of 100

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				Date	Monday, July 15, 2019	Sheet 71 of 100
				LA-H451P		
				1.0		

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				Date	Monday, July 15, 2019	1.0
				Sheet	72 of 100	



CIO6
Main : SE00000FWY0
2nd : SE00000FWW0

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				LA-H451P	1.0
Date: Monday, July 15, 2019				Sheet	73 of 100

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				Date	Monday, July 15, 2019	1.0
				Sheet	74 of 100	

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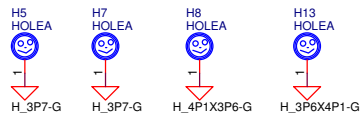
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				Date	Monday, July 15, 2019	1.0
				Sheet	75 of 100	

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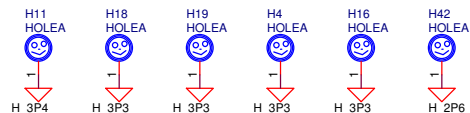
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Issued Date	2018/08/31	Deciphered Date	2019/08/06	Title	Reserve	
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					LA-H451P	1.0
				Date:	Monday, July 15, 2019	Sheet 76 of 100

Main Func = Screw

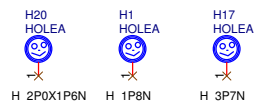
CPU & GPU



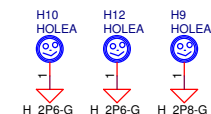
Stand-off



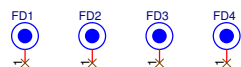
NPTH



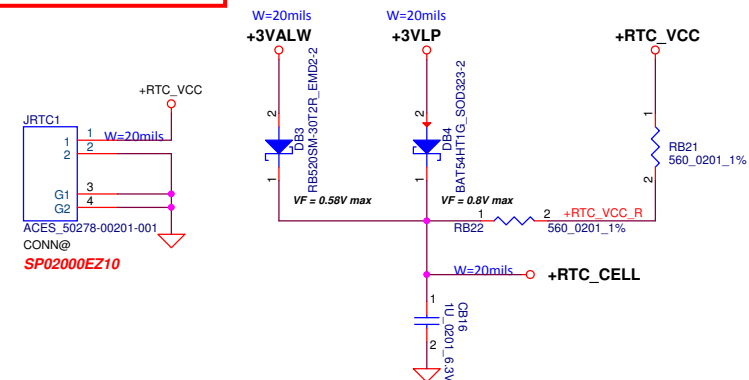
PTH



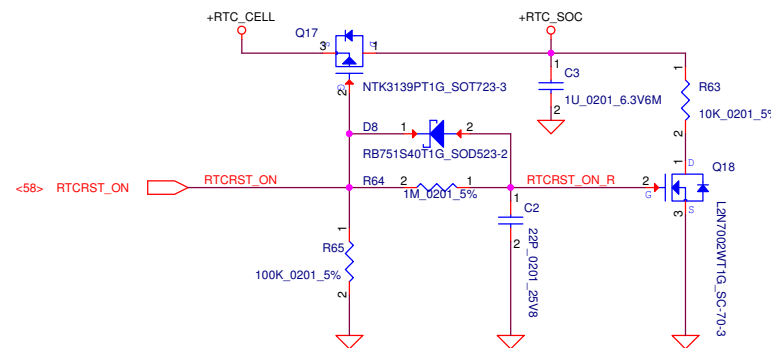
FD



Main Func = RTC

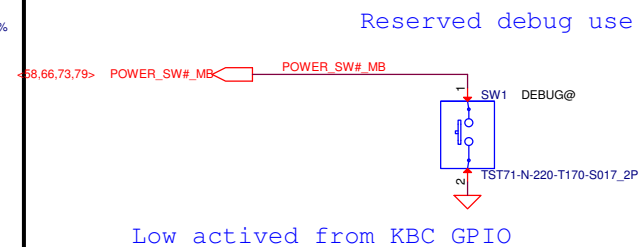


RTC power gating circuit

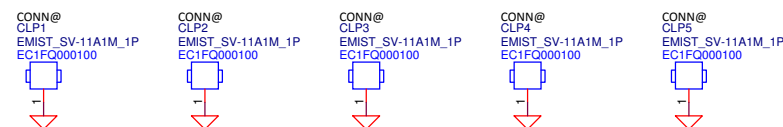


Main Func = Power BTN

On IO Board



Clip x 5



Shielding Frame X 9 (NPTH)



zzz
PCB R1
DAA000IZ000
PCB@
PCB 2KD LA-H451P REV0 M/B

PCB R3

CPU R1
UC1
SA0000C6R0L
WHL_I3_QS@
S IC A31 FJ8068404064702 QQK9 W0 2.1G

CPU R3
UC1
SA0000C6R3L
WHL_I3_MP@
S IC FJ8068404064702 SRD1V W0 2.1G A31!

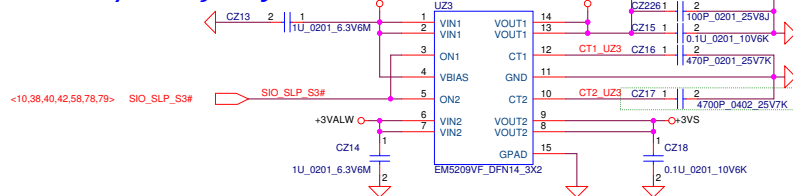
UC1
SA0000C6P0L
WHL_I7_QS@
S IC A31 FJ8068404064403 QQK6 W0 1.8G

UC1
SA0000C6Q3L
WHL_I5_MP@
S IC FJ8068404064604 SREJQ W0 1.6G A31!

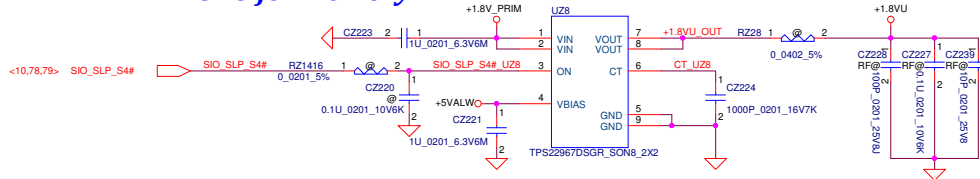
UC1
SA0000C6P2L
WHL_I7_MP@
S IC FJ8068404064405 SREJP W0 1.8G A31!

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				Date	Monday, July 15, 2019
				Sheet	77 of 100

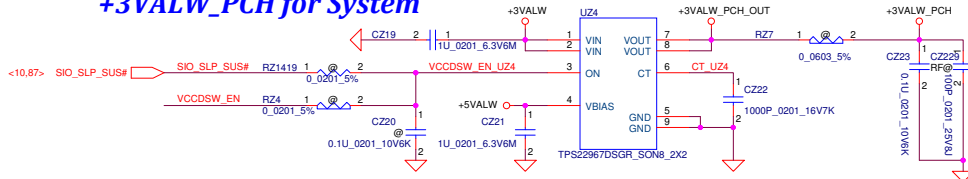
+5VS/+3VS for System



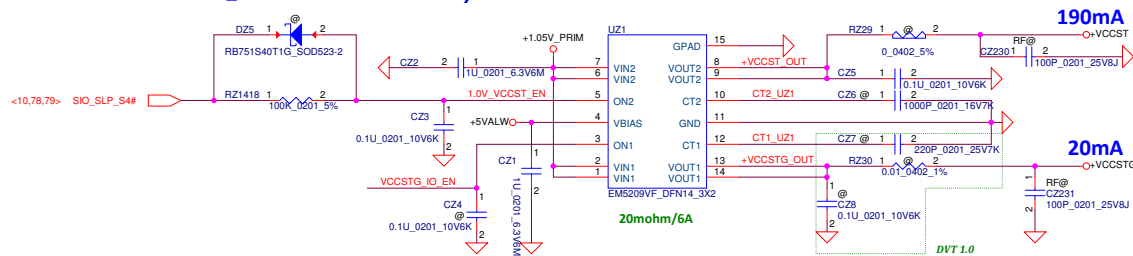
+1.8VU for Memory



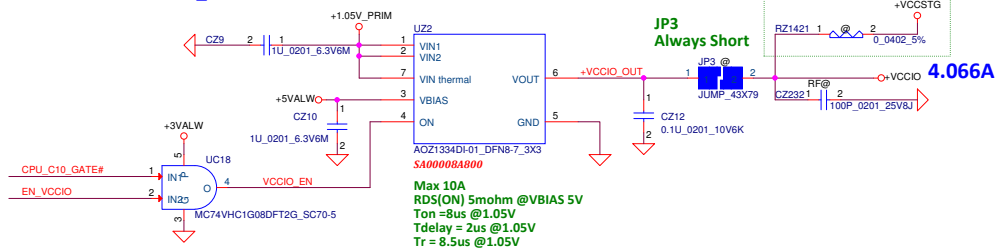
+3VALW_PCH for System



+1.05V_PRIM TO +VCCST/+VCCSTG

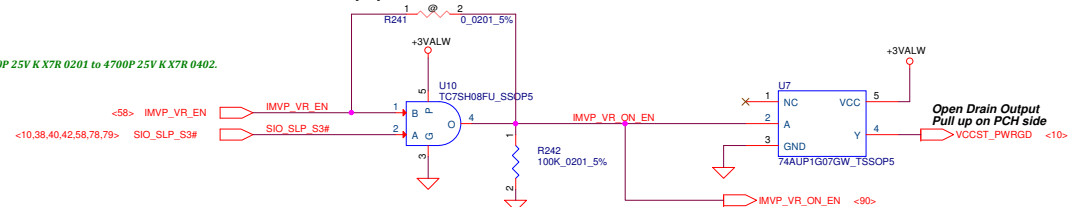


+1.05V_PRIM TO +VCCIO



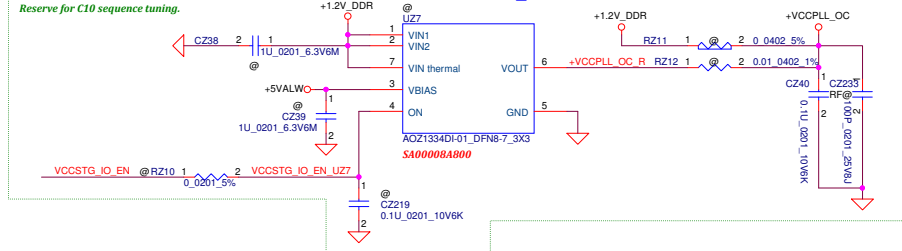
IMVP_VR_ON & VCCST_PWRGD

If popR241,R242 need NC



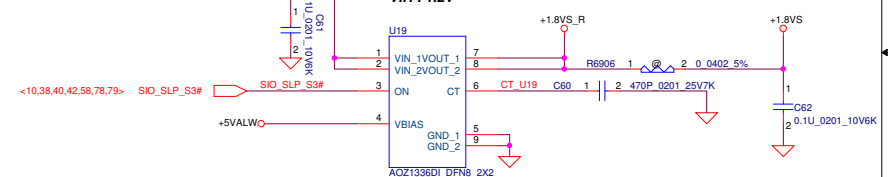
DVT 1.0
Add CZ38, CZ39, CZ219, RZ10, RZ12, UZ7 un-pop(@).
Reserve for C10 sequence tuning.

+VCCPLL_OC source



Max Current : 4A
RON : 30m ohm
VIH : 1.2V

1.8VS



<58,87,89> VCCDSW_EN VCCDSW_EN

<10,84,85> POK

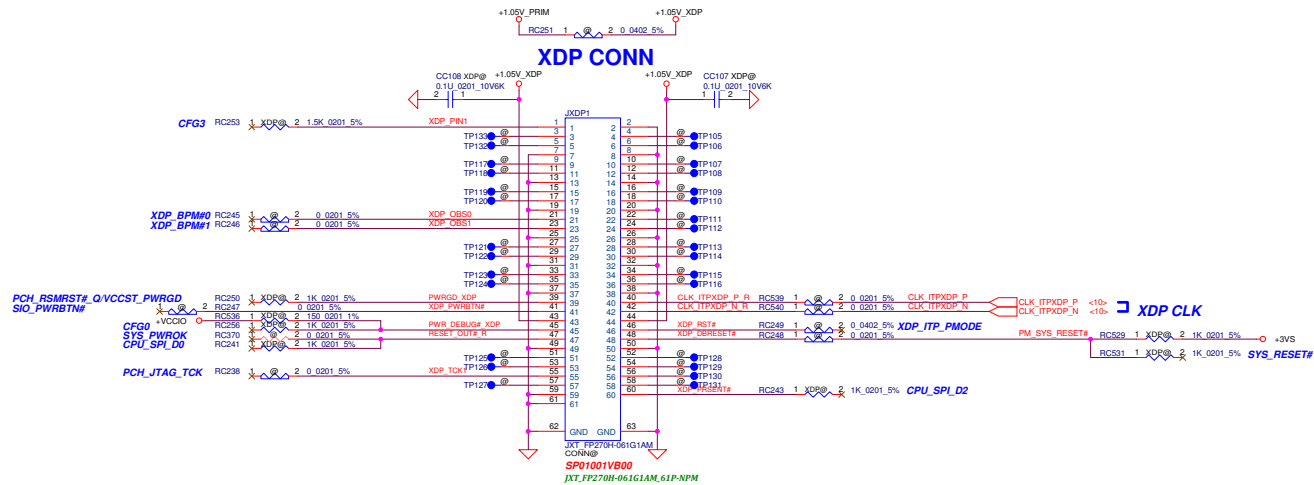
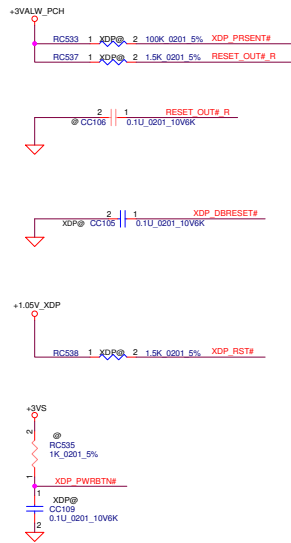
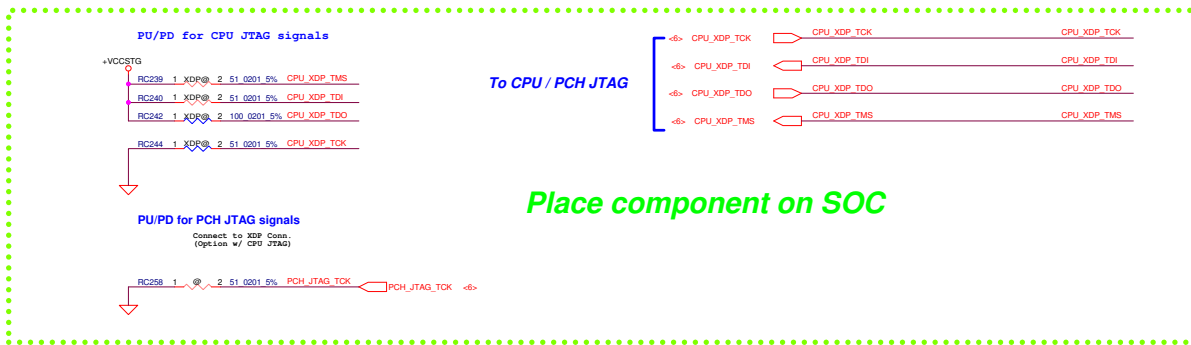
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<10,78,79> SIO_SLP_S4#  SIO_SLP_S4#

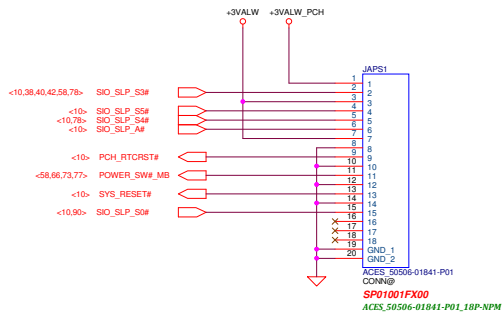
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						Document Number	Rev
						LA-H451P	1.0
Date: Monday, July 15, 2019						Sheet 78 of 100	

Main Func = XDP



Main Func = APS debug



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Issued Date	2018/08/31	Deciphered Date	2019/08/06	Title	XDP
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				Date	Monday, July 15, 2019
				Sheet	79 of 100

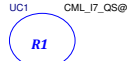
CPU



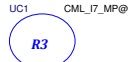
S IC A31 CL8068404064503 QRYX V0 1.6G
SA0000CNQ0L



S IC A31 CL8068404064305 QRYX V0 1.9G
SA0000CNP0L



S IC A31 FJ8070104303905 QSBF V0 1.8G S
SA0000CU20L



S IC FJ8070104303905 SRGW V0 1.8G A31!
SA0000CU21L

GPU



S IC N17S-G2-A1 BGA 595P GPU A31 I,
SA0000CB0L



S IC A31 FJ8070104307504 QSBG V0 1.6G S
SA0000CT1L



S IC FJ8070104307504 SRGY V0 1.6G A31!
SA0000CT2L

LPDDR3 Micron 4GB



MT52L256M32D1PF-093WT:B_FBGA178
SA0000AZU0L



MT52L256M32D1PF-093WT:B_FBGA178
SA0000AZU0L



MT52L256M32D1PF-093WT:B_FBGA178
SA0000AZU0L



MT52L256M32D1PF-093WT:B_FBGA178
SA0000AZU0L

LPDDR3 Micron 8GB



MT52L512M32D2PF-093WT:B_FBGA178
SA0000AM40L



MT52L512M32D2PF-093WT:B_FBGA178
SA0000AM40L



MT52L512M32D2PF-093WT:B_FBGA178
SA0000AM40L



MT52L512M32D2PF-093WT:B_FBGA178
SA0000AM40L

LPDDR3 Micron 16GB



MT52L1G32D4PG-093WT:B_FBGA178
SA00009ZN1L



MT52L1G32D4PG-093WT:B_FBGA178
SA00009ZN1L



MT52L1G32D4PG-093WT:B_FBGA178
SA00009ZN1L



MT52L1G32D4PG-093WT:B_FBGA178
SA00009ZN1L

LPDDR3 Hynix 4GB



H9CCNNN8GTALAR-NVD_FBGA178
SA0000AZR1L



H9CCNNN8GTALAR-NVD_FBGA178
SA0000AZR1L



H9CCNNN8GTALAR-NVD_FBGA178
SA0000AZR1L



H9CCNNN8GTALAR-NVD_FBGA178
SA0000AZR1L

LPDDR3 Hynix 8GB



H9CCNNNBJTALAR-NVD_FBGA178
SA0000ALP1L



H9CCNNNBJTALAR-NVD_FBGA178
SA0000ALP1L



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SA0000ALP1L



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SA0000ALP1L

LPDDR3 Hynix 16GB



H9CCNNNCLGALAR-NVD_FBGA178
SA00009ZL1L



H9CCNNNCLGALAR-NVD_FBGA178
SA00009ZL1L



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SA00009ZL1L



H9CCNNNCLGALAR-NVD_FBGA178
SA00009ZL1L

Model ID



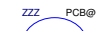
For Model ID Select
UMA 10K
DIS 17.8K

Board ID



For Board ID Select
Pre-EVT 10K
EVT 17.8K
DVT1 37.4K
DVT1.1 49.9K
DVT2 64.9K
Pilot 107K

PCB



PCB 2KD LA-H451P REV0 M/B
DAA000IZ000

Phase ID



VRAM Micron 2G



MT51J256M32HF-80:B
SA00009T13L



MT51J256M32HF-80:B
SA00009T13L

VRAM Hynix 2G



H5GC8H24AJR-R2C
SA0000C171L



H5GC8H24AJR-R2C
SA0000C171L

RAM_CFG	STRAP2	STRAP1	STRAP0
M2G 0x09 (LML)	RV388 N17M2G@	RV390 N17M2G@ RV51 N17M2G@	RV383 N17M2G@
H2G 0x0A (LMH)	RV388 N17H2G@	RV390 N17H2G@ RV51 N17H2G@	RV384 N17H2G@

LPDDR3 Samsung 4GB



K4E8E324EB-EGCG_FBGA178
SA0000BTE1L



K4E8E324EB-EGCG_FBGA178
SA0000BTE1L



K4E8E324EB-EGCG_FBGA178
SA0000BTE1L



K4E8E324EB-EGCG_FBGA178
SA0000BTE1L

LPDDR3 Samsung 8GB



K4E6E304EC-EGCG_FBGA178
SA0000AZT2L



K4E6E304EC-EGCG_FBGA178
SA0000AZT2L



K4E6E304EC-EGCG_FBGA178
SA0000AZT2L



K4E6E304EC-EGCG_FBGA178
SA0000AZT2L

LPDDR3 Samsung 16GB



K4E6E304EC-EGCG_FBGA178
SA00008YV3L



K4E6E304EC-EGCG_FBGA178
SA00008YV3L



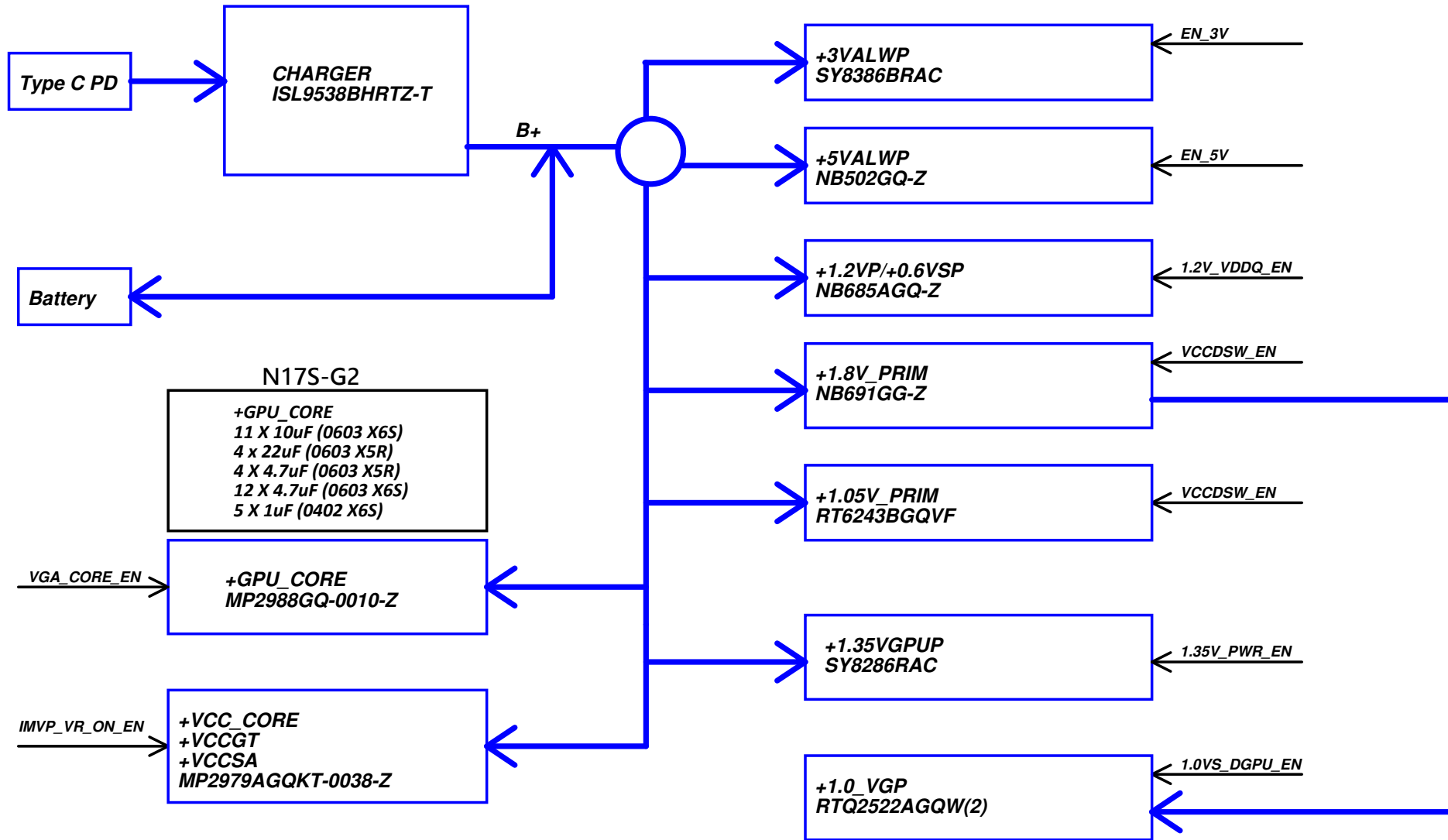
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SA00008YV3L



K4E6E304EC-EGCG_FBGA178
SA00008YV3L

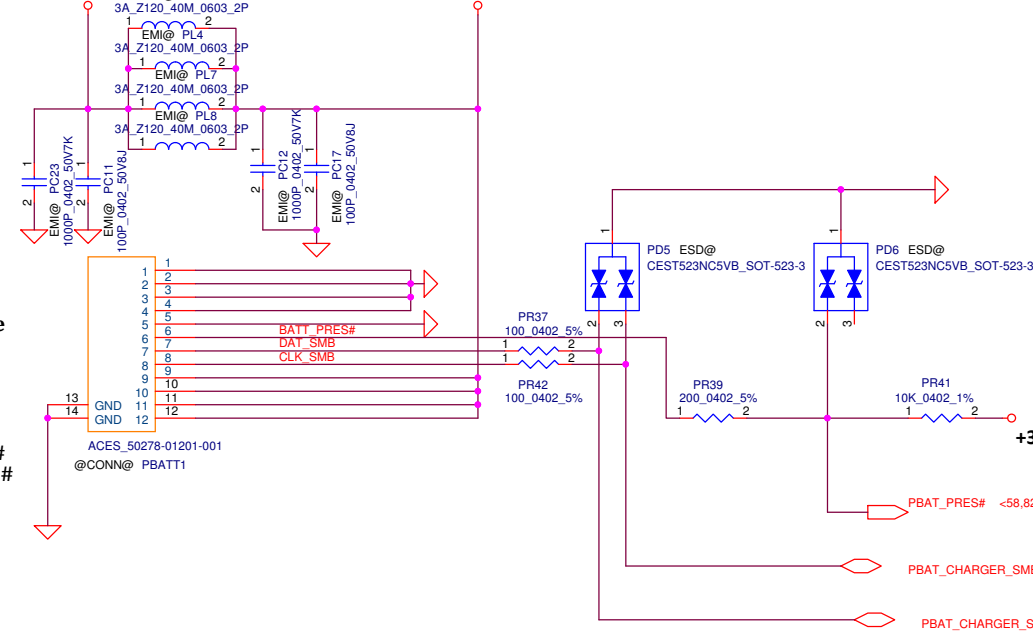
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Issued Date	2018/08/31	Deciphered Date	2019/08/06	Compal Electronics, Inc.	
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				Document Number	Rev 1.0
				LA-H451P	
				Date: Monday, July 15, 2019	Sheet 80 of 100

Power block



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				Date:	Monday, July 15, 2019
				Sheet	81 of 100

+8.4V_BATT +8.4V_BATT+

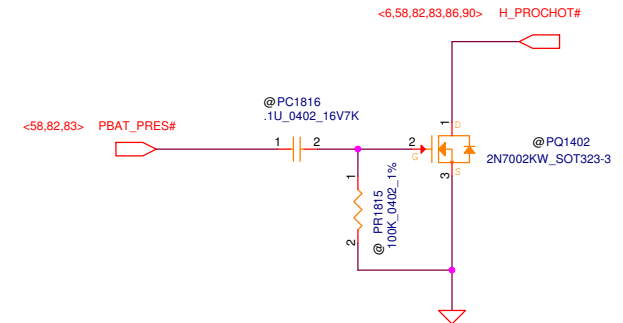


Battery Bot Side

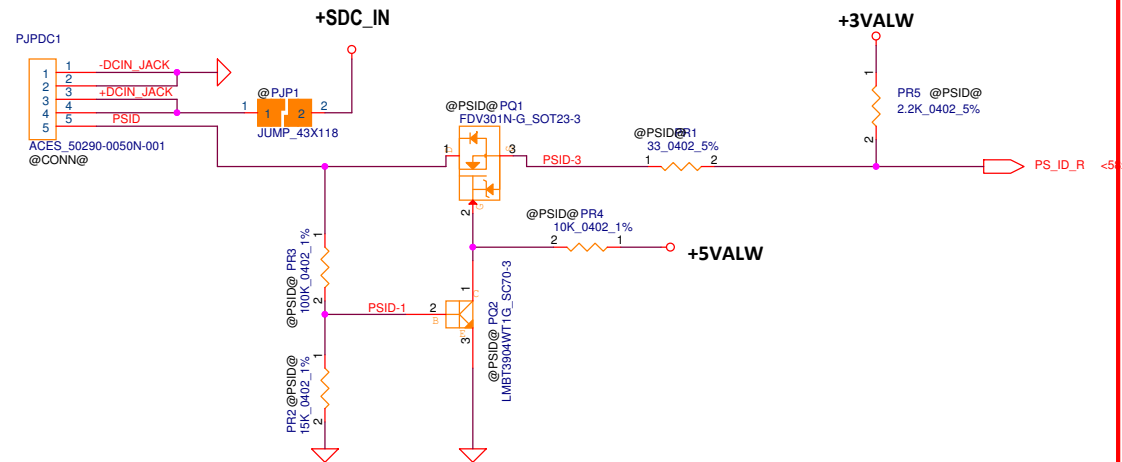
PIN1 GND
PIN2 GND
PIN3 GND
PIN4 GND
PIN5 SYS_PRES#
PIN6 BATT_PRS#
PIN7 DAT_SMB
PIN8 CLK_SMB
PIN9 BATT+
PIN10 BATT+
PIN11 BATT+
PIN12 BATT+
SP011603251
ACES_50278-01201-001

Adapter protection:

asserts H_PROCHOT# when adaptor is unplugged, keep low for 10ms till SW PROCHOT# is issued by EC

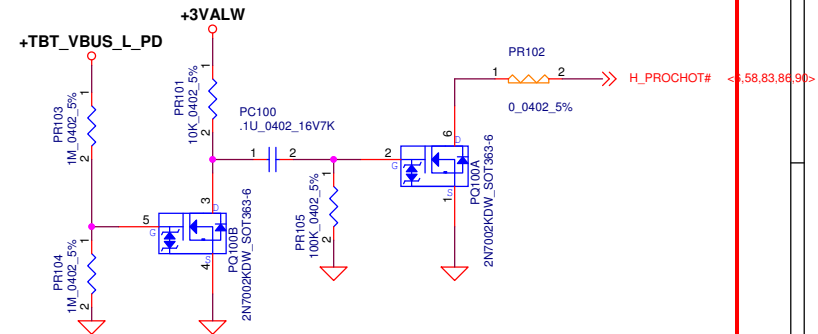


DC IN:

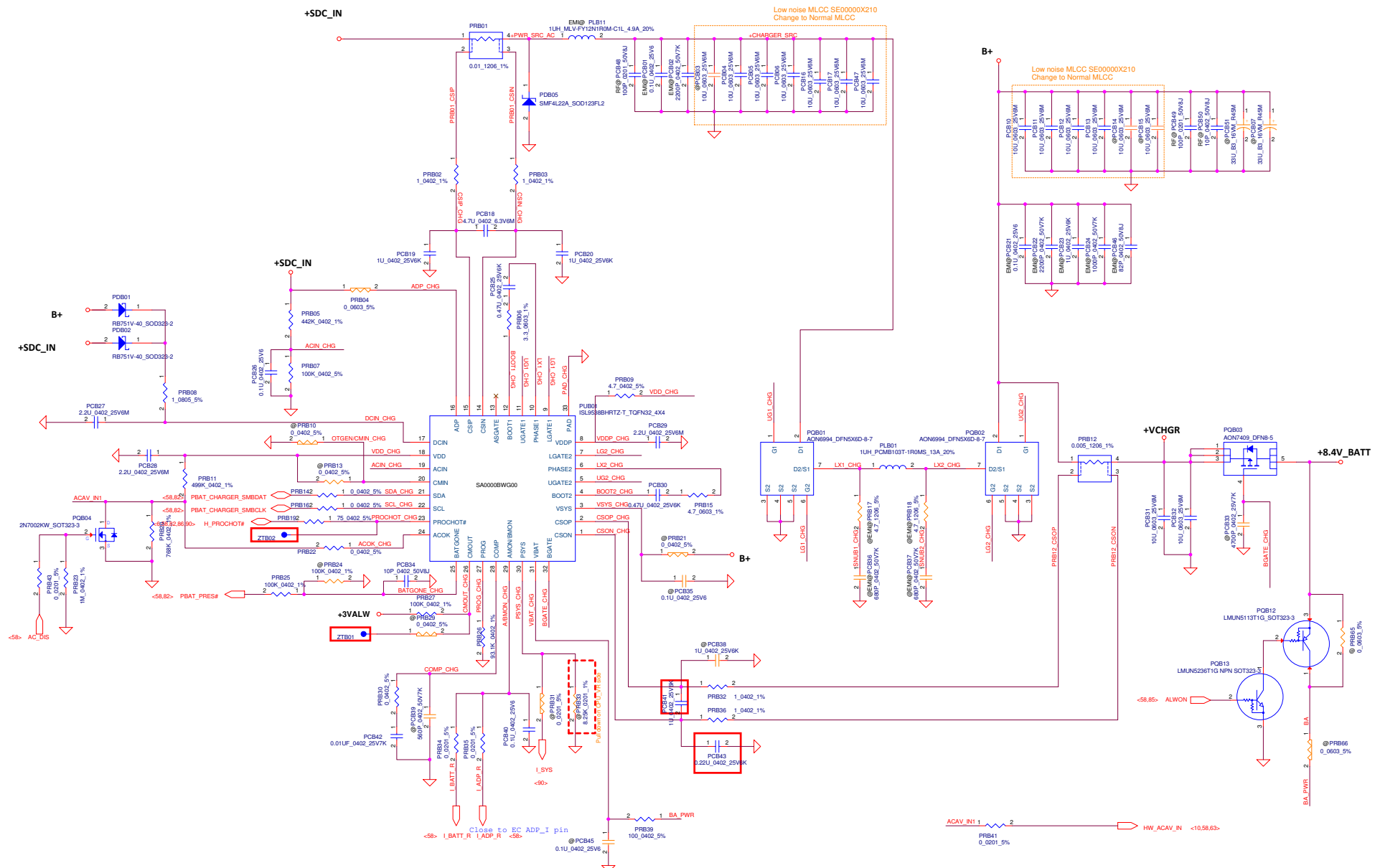


Battery protection:

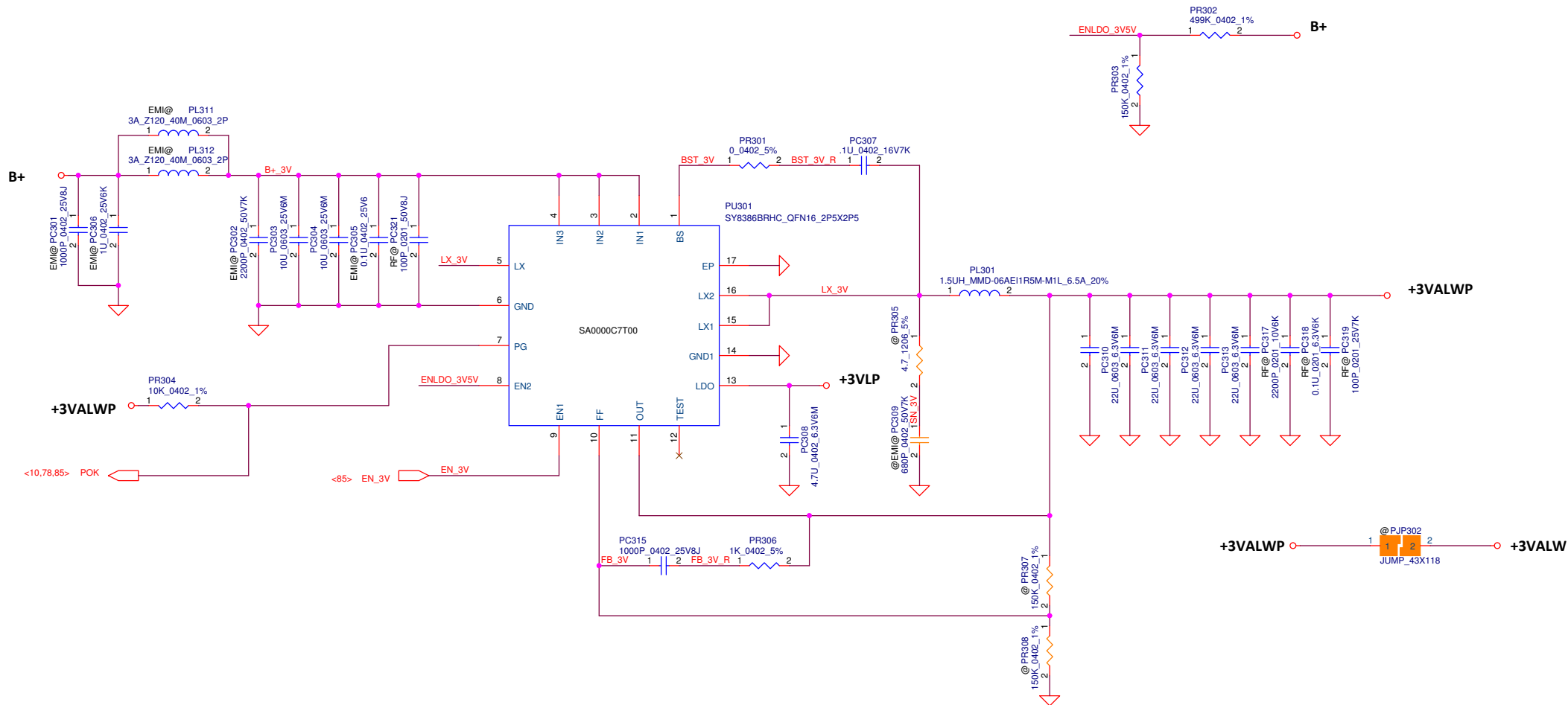
asserts H_PROCHOT# when TypeC is unplugged, keep low for 10ms till SW PROCHOT# is issued by EC



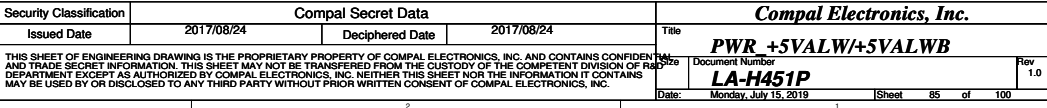
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Issued Date	2017/08/24	Deciphered Date	2017/08/24	Title	PWR DCIN
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				Date	Monday, July 15, 2019
				Sheet	82 of 100
				Rev	1.0



+3VALWP
TDC 5.85A
Peak Current 9.74 A
OCP Current 9.15A
Fsw 600K Hz

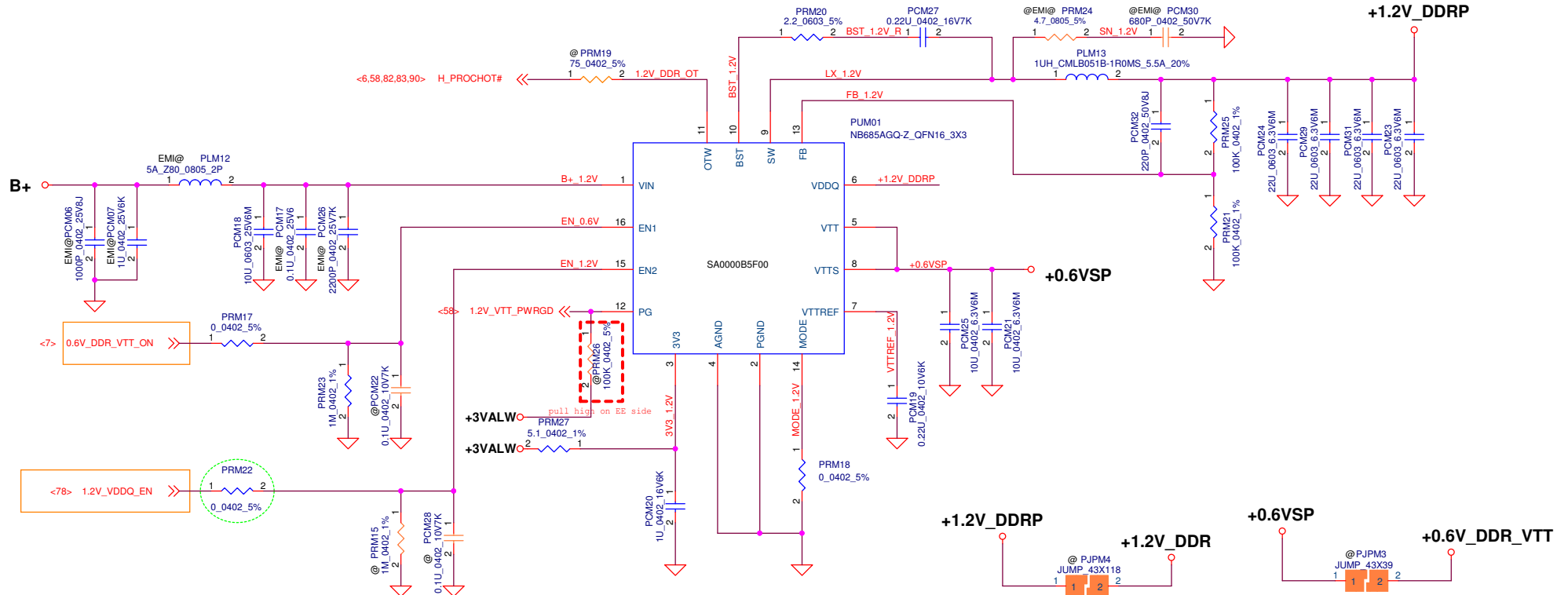


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				Date:	Monday, July 15, 2019
				Sheet	84 of 100
				Rev	1.0



DDR controller(35.3), Support component(35.4)

Main: CYN, 2nd: CLSN
Package: 5.4 x 5.7 x 1.2
Idc=5.5A, Isat=8.7A
DCR=26mohm (Typ.)



Mode	EN1	EN2	VDDQ	VTT
S0	H	H	on	on
S3	L	H	on	off
S4/S5	L	L	off	off

Note: S3 - sleep ; S5 - power off

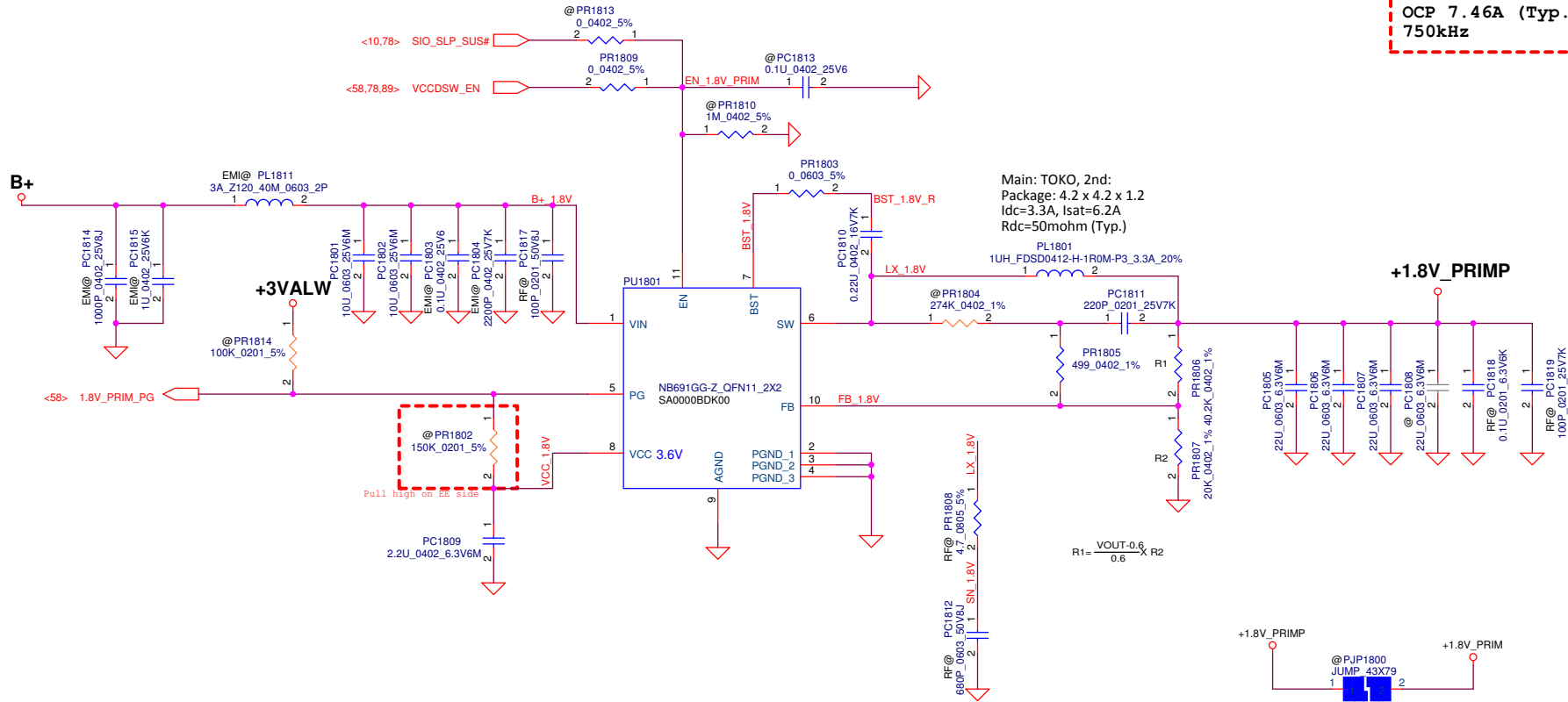
Note: S3 - sleep ; S5 - power off

State	USM	Fs	Resistor to GND
M1	NO	700 KHz	0
M2	Yes	700 KHz	90K
M3	NO	500 KHz	150K
M4	Yes	500 KHz	>230K or float

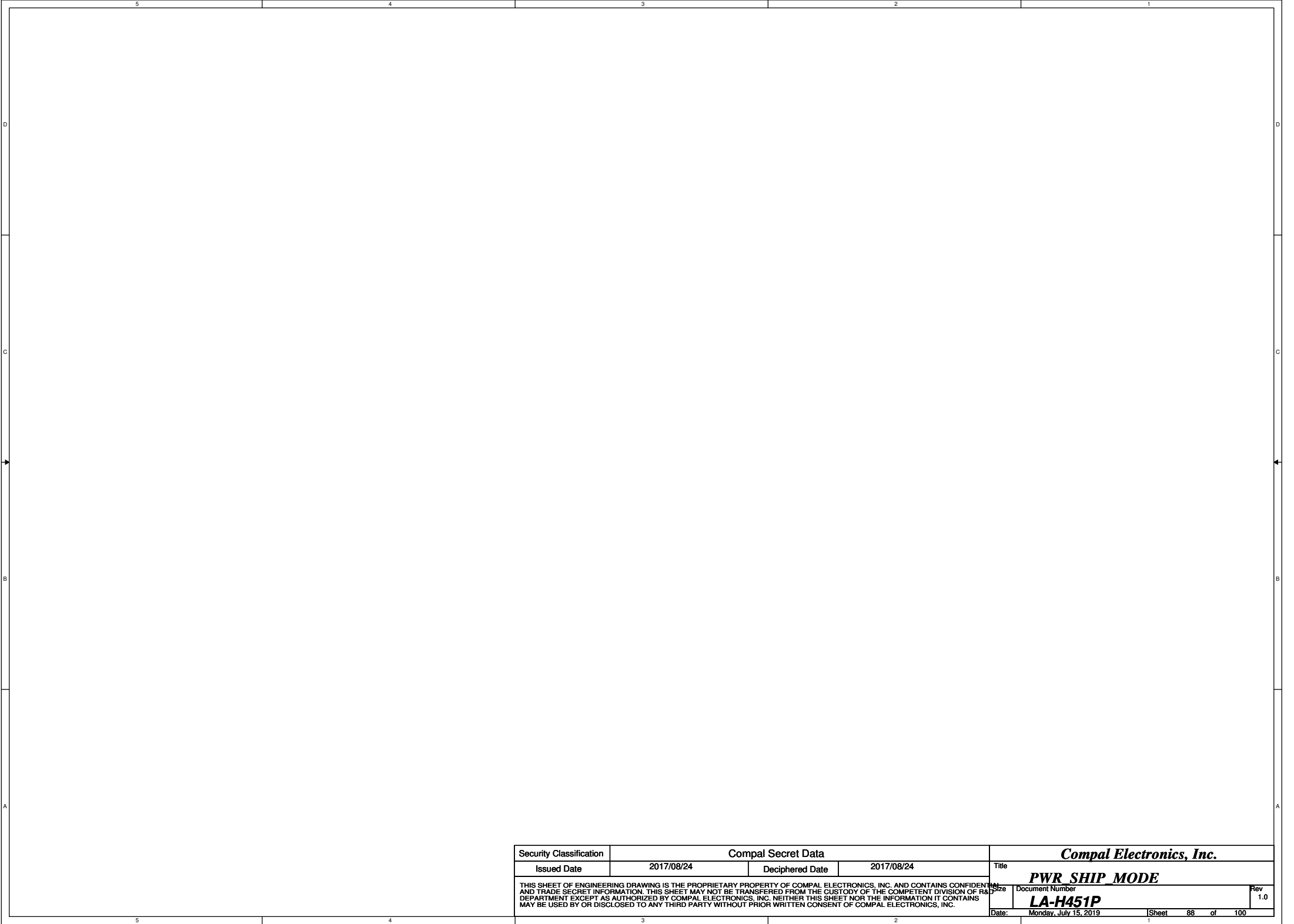
```
+1.2V_DDR
TDC 4.44A
Peak Current 6.35A
OCP Current 12.75A
Frequency 700KHz
```

```
+0.6VS
TDC 0.28A
Peak Current 0.4A
OCP Current 1.59A
Frequency 700KHz
```

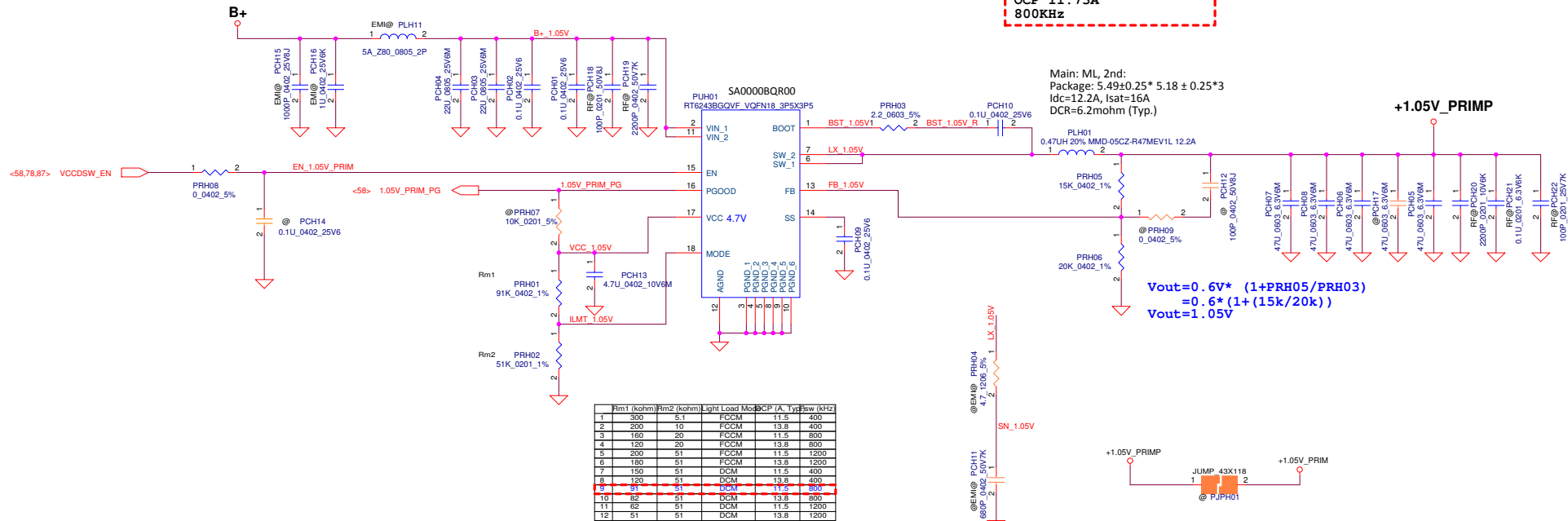
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					LA-H451P	1.0
				Date: Monday, July 15, 2019	Sheet 86 of 100	



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				Date	Monday, July 15, 2019
				Sheet	87 of 100
				Rev	1.0



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					LA-H451P	1.0
Date: Monday, July 15, 2019				Sheet	88	of 100



+1.05VAP
TDC 6.3A
Peak Current 9A
OCF 11.73A
800KHz

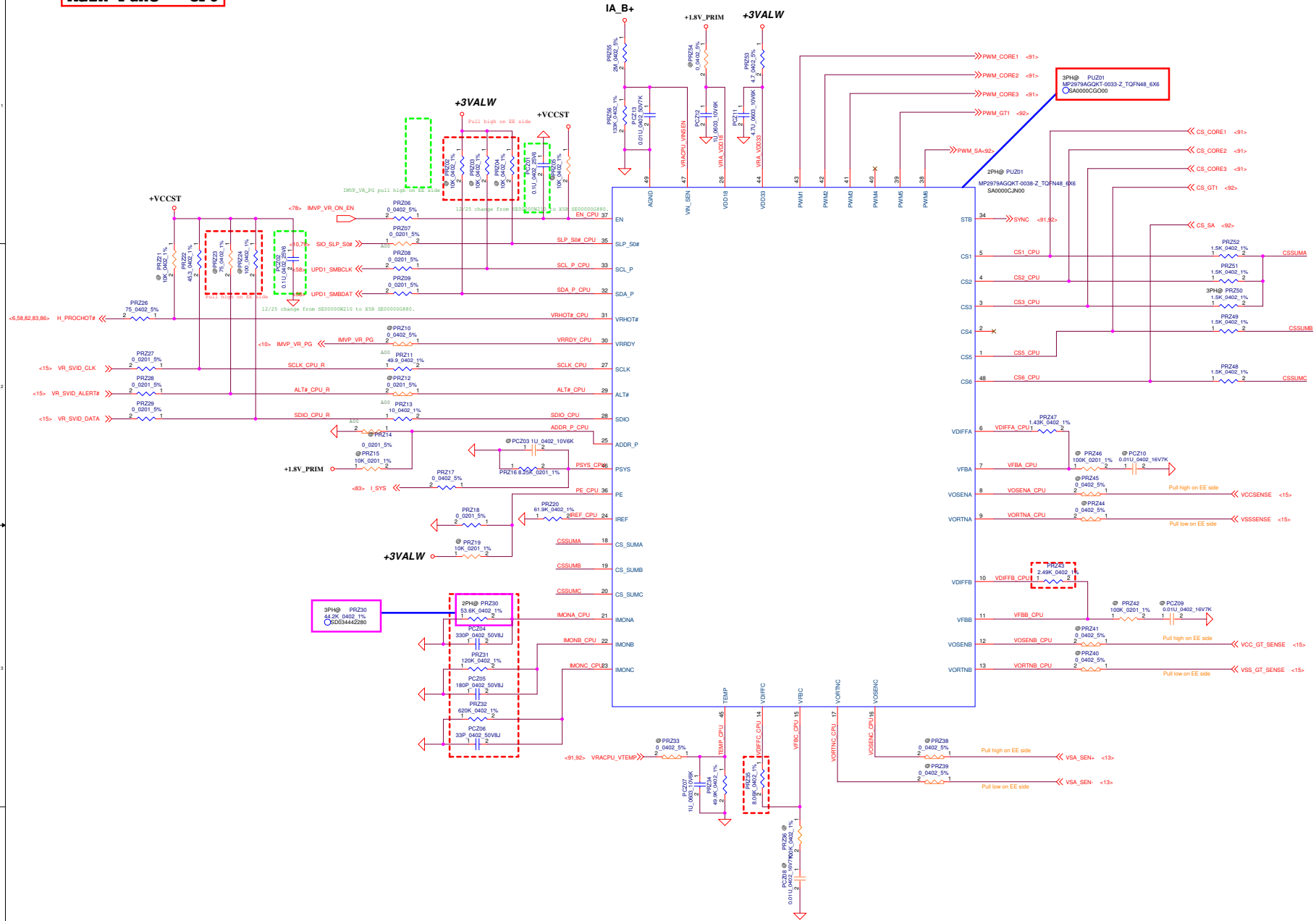
Main: ML, 2nd:
 Package: 5.49±0.25* 5.18 ± 0.25*3
 Idc=12.2A, Isat=16A
 DCR=6.2mohm (Typ.)

$$V_{out} = 0.6V * (1 + PRH05 / PRH03)$$

$$= 0.6 * (1 + (15k / 20k))$$

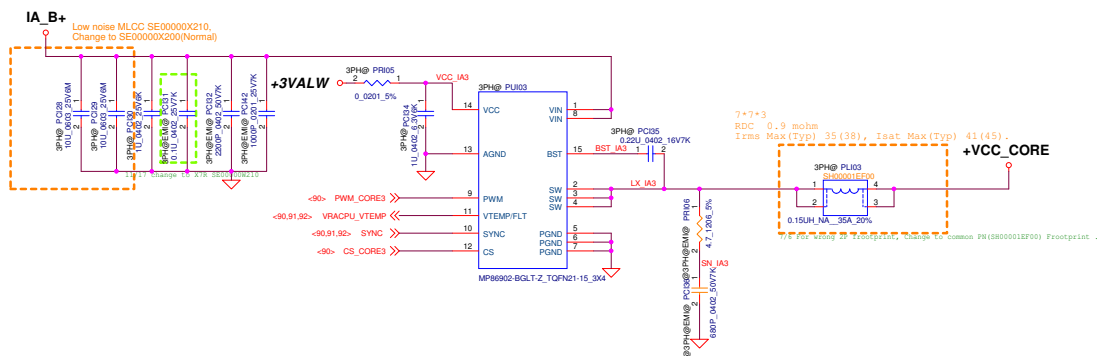
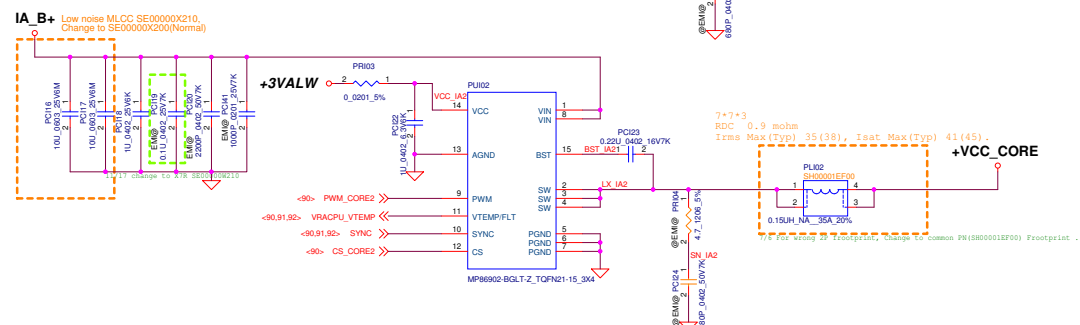
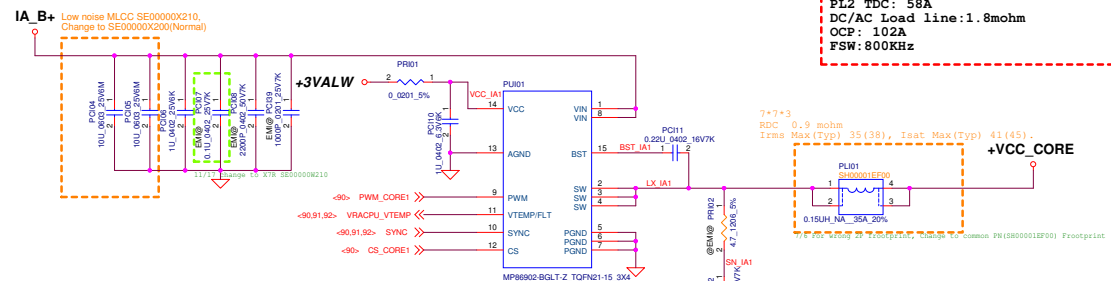
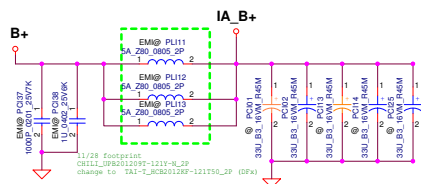
$$V_{out} = 1.05V$$

Main Func = CPU



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				PWR-VCORE
			Date:	Monday, July 15, 2019
			Sheet	99 of 100
			Rev	1.0

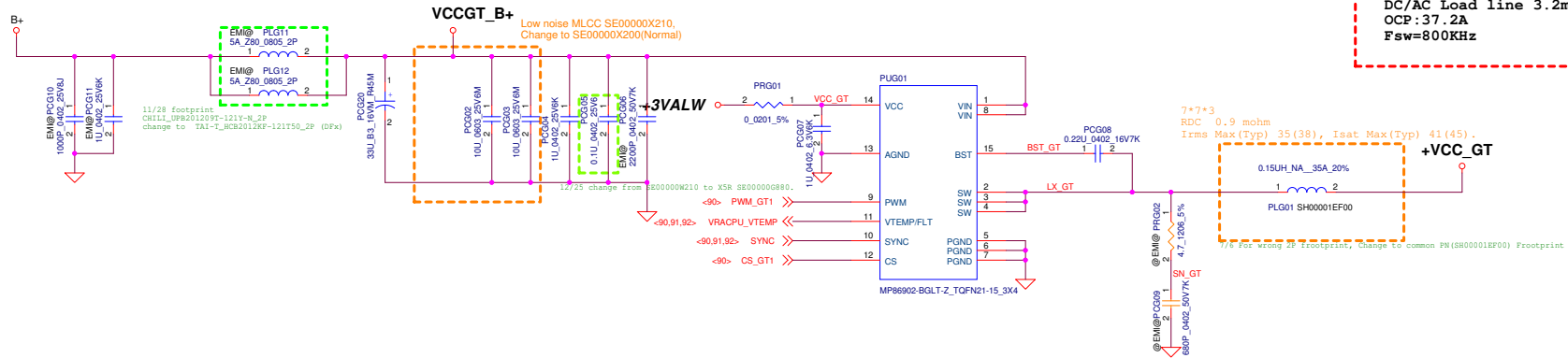
VCC_CORE Dr. MOS (36.2), Support component(36.3)



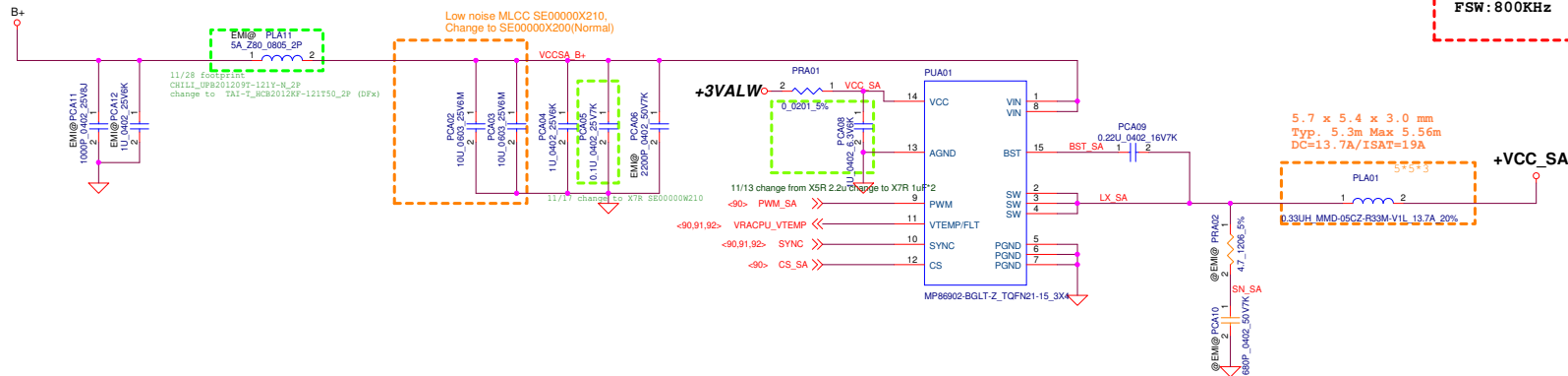
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Date	Monday, July 15, 2019	ISheet	91	1.00

VCC_GT/SA Dr. MOS (36.2), Support component(36.3)

VCCGT(Base on CML_U42 Pref
PL2 TDC Max: 18A
Max current:31A
DC/AC Load line 3.2mohm
OCP:37.2A
Fsw=800KHz



VCCSA(Base on CML_U42 Pref
PL2 TDC Max: 6A
Max current:10.3A
DC/AC Load line 10.3mohm
OCP:12.36A
FSW:800KHz



Main Func = IA / GT / SA MLCC

+VCC CORE

+VCC GT

+VCC_SA

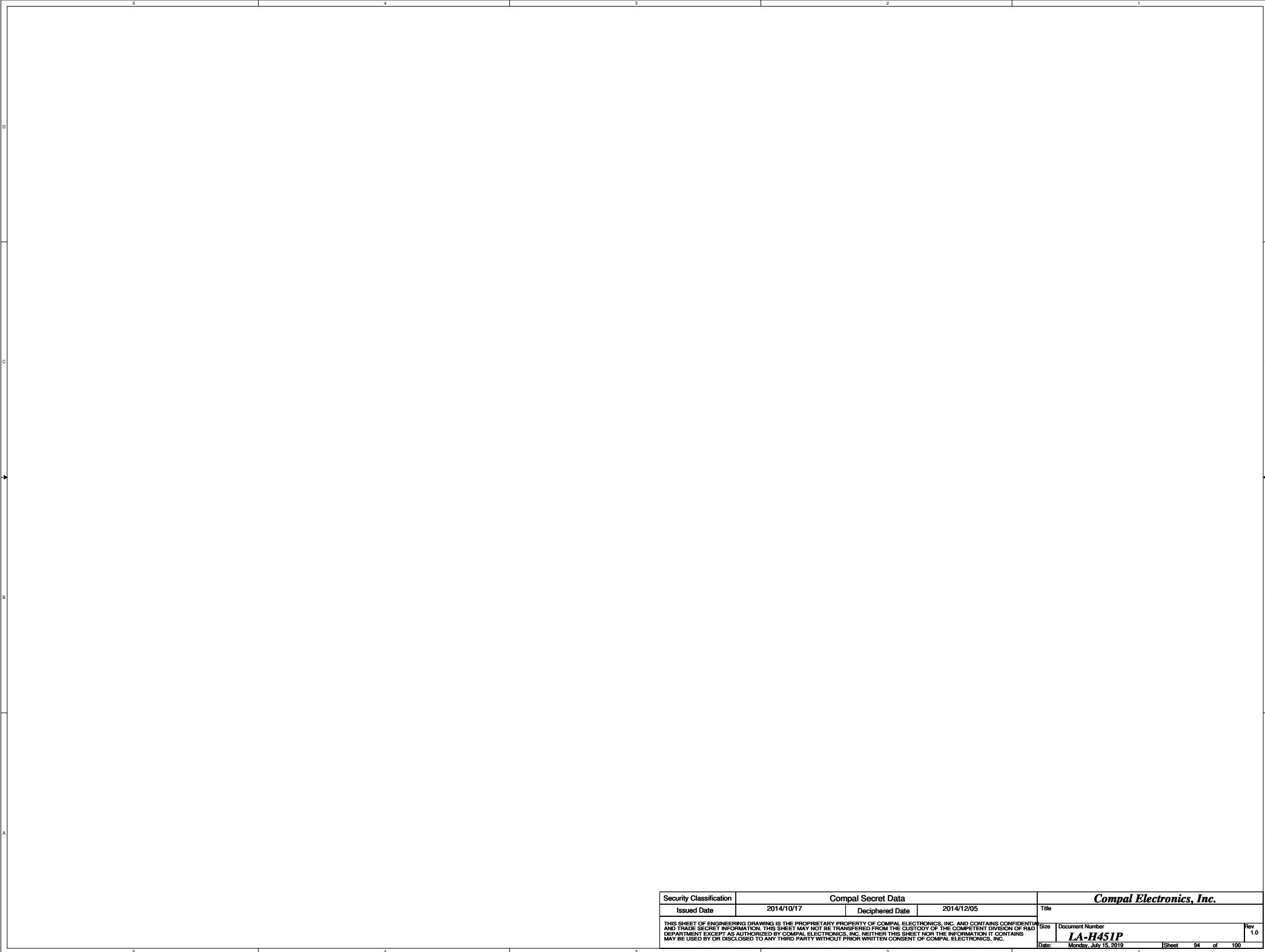
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					PWR-CPU Decoupling CAP
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					Rev
					1.0
Date:		Monday, July 15, 2019	Sheet	93	of 100

Low noise MLCC SE00000M0M0 H=0.8mm,
Change to Normal MLCC

low noise cap_H=0.8 (TOP) *10

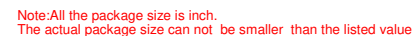
Low noise MLCC SE00000M0M0 H=0.8mm,
Change to Normal MLCC

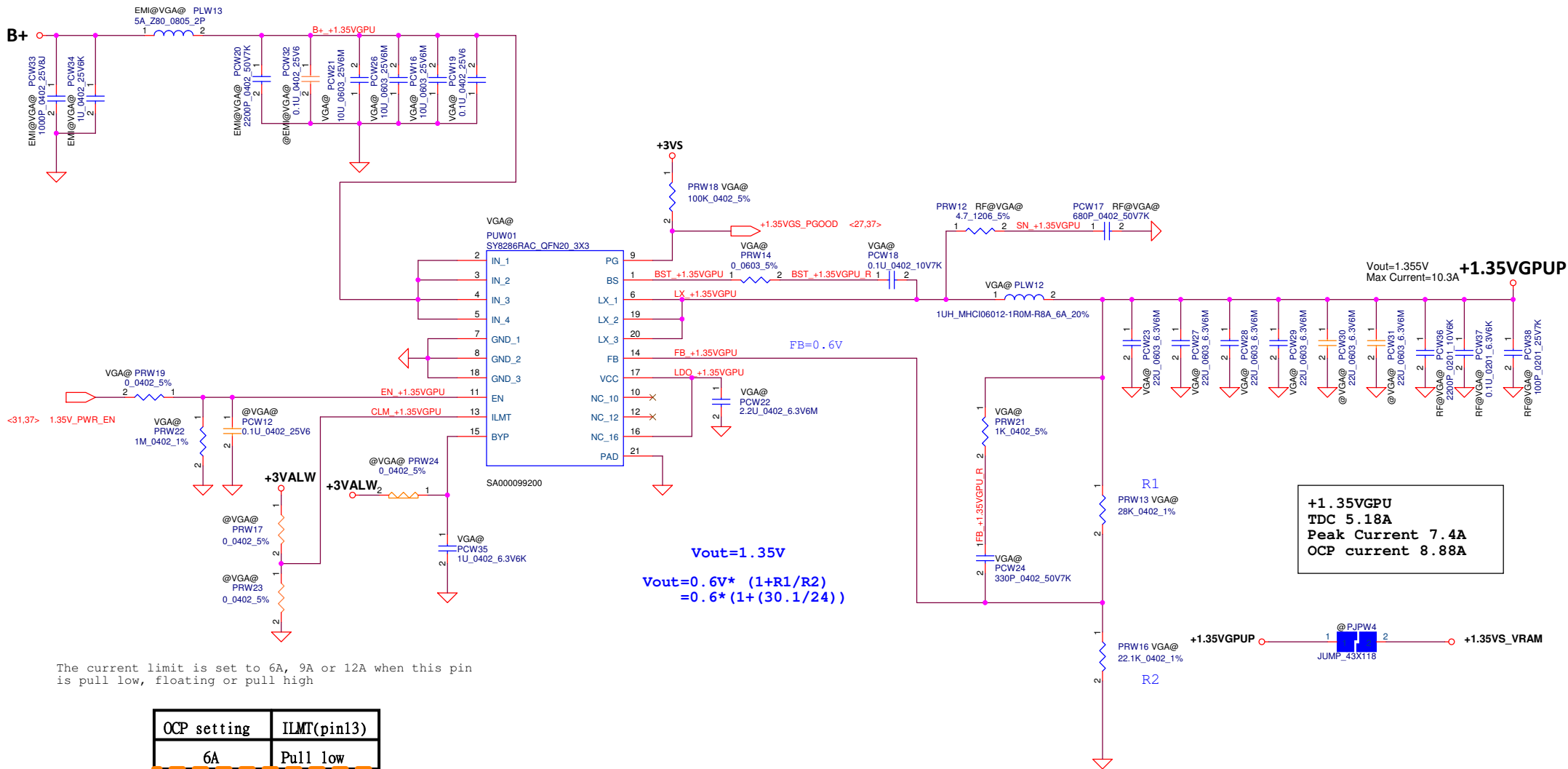
low noise cap_H=0.8 *8

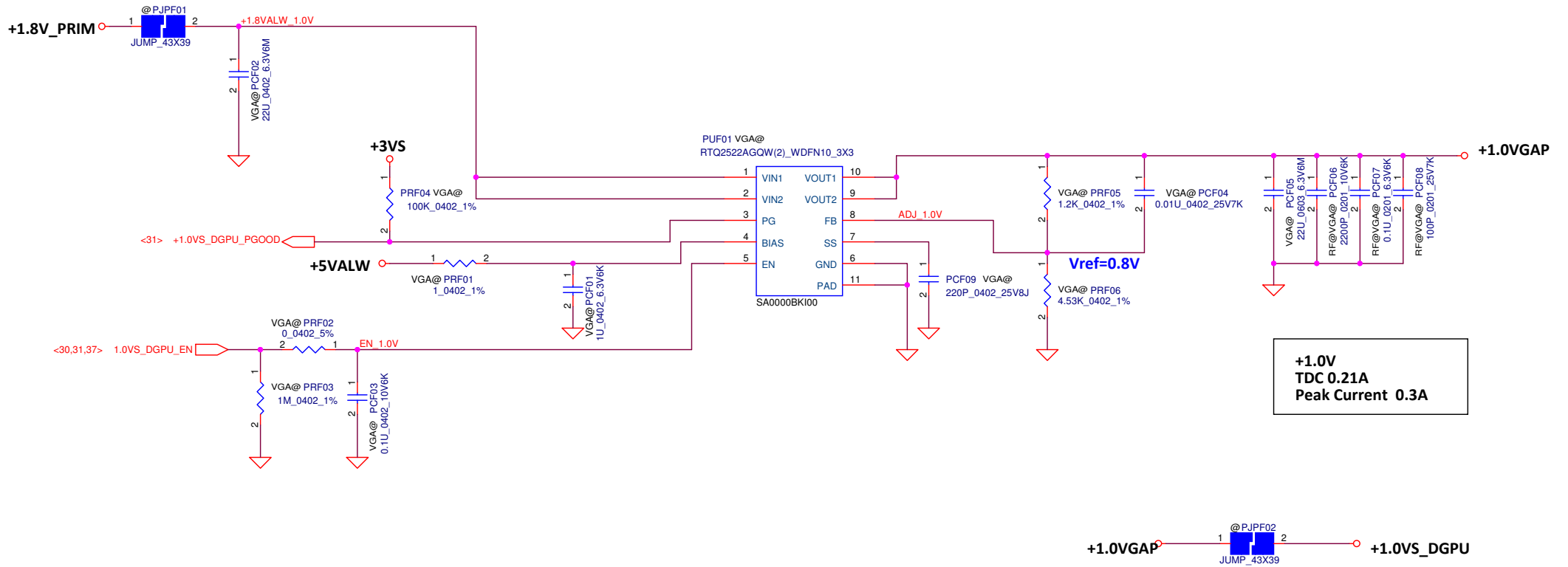


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					LA-H451P
				Date:	Monday, July 15, 2019
				Sheet	94 of 100
				Rev	1.0

Controller --- MP2988







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Date: Monday, July 15, 2019				Sheet	97 of 100

Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1							
2							
3							
4							
5							
6							
7							
8							
9							
10							
11							
12							
13							
14							
15							
16							
17							
18							

Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1							
2							
3							
4							
5							
6							
7							
8							
9							
10							
11							
12							
13							
14							
15							
16							
17							
18							

Item	Page#	Title	Date	Request	Owner	Issue Description	Solution Description	Rev.
1	73							
2	61							
3	69							
4	71							
5	59							
6	59							
7	59							
8								
9								
10								
11								
12								
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15								
16								
17								
18								

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				Date: Monday, July 15, 2019	Sheet 100 of 100